

PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

Dutton/Jett Block Diagram -- Intel Chief River ULV

POWER

DC/DC 3VPCU, 5VPCU, +15V	Page 31
REGULATOR (DDR3) 1.5VSUS, +0.75V_DDR_VTT	Page 32
REGULATOR +1.05V&+1.8V	Page 33,34
REGULATOR +VCCSA	Page 35
CPU Core +VCC_CORE&+VCC_GFX	Page 36
Charger VIN	Page 37
RUN POWER SW/Discharge 3VSUS, 5VSUS, 3V_S5, 5V_S5, +3V, +5V	Page 38

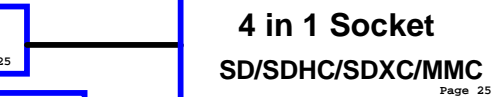
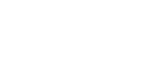
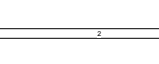
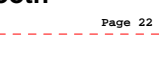
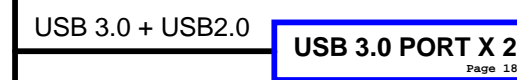
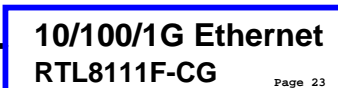
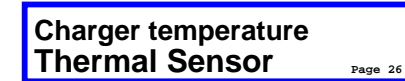
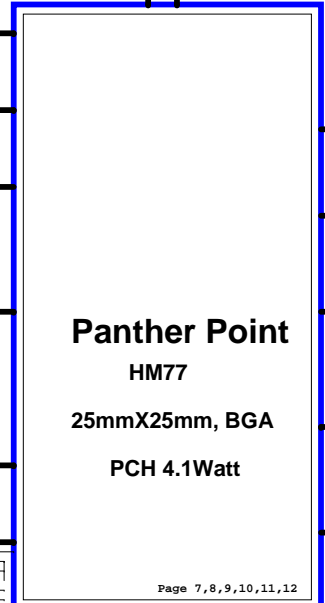
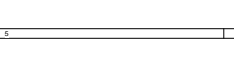
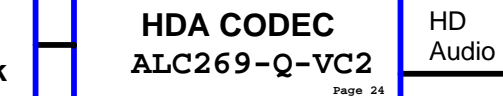
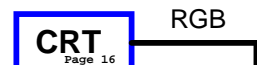
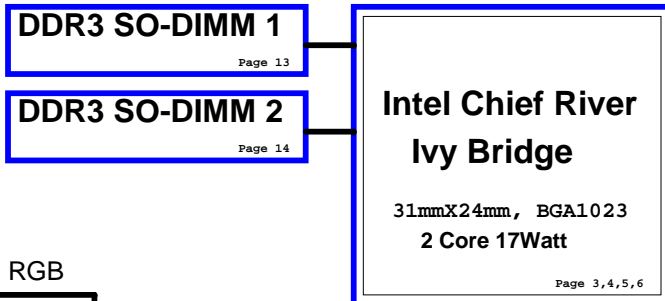


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Power States

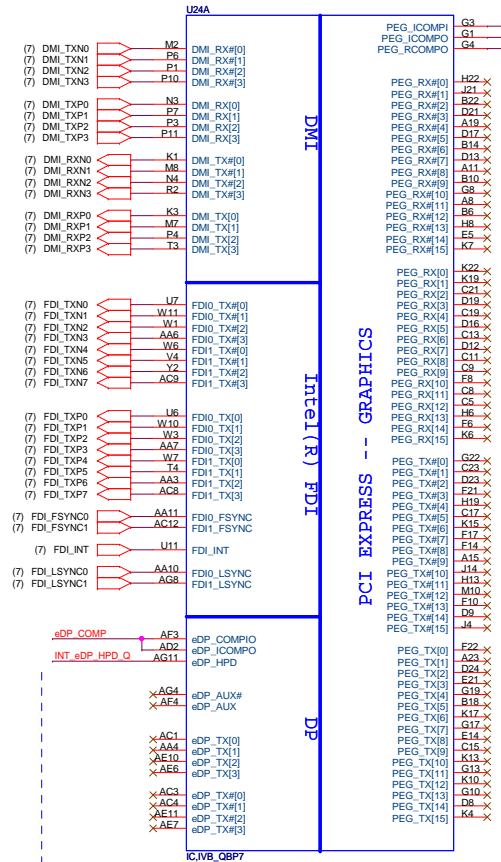
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,31,32,33,34,35,36,37	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,28	RTC		S0~S5
3VPCU	+3.3V	8,15,16,17,20,27,28,31,33,36,37	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	15,29,31,32,33,34,36,37	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	15,25,31,32,37	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	17,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,20,37	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,22,25,27,28,37	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	15,27,35,37	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	32,37	SLP_S4# CTRLD POWER	SUSON	S0~S3
+1.5VSUS	+1.5V	3,11,13,14,32,37	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,32,37	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,15,16,18,19,24,26,28,29,37	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,16,17,18,19,21,22,23 24, 25,26,27,28,29	SLP_S3# CTRLD POWER	MAINON	S0
+VCC_GFX		5,35,37	VGA CORE POWER	MAINON	S0
+VCCSA	+0.8V~+0.9V	5,34,37	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,33,37	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,33,37	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_CORE		5,6,35,37	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	ENVDD	S0
+3V_HDD	+3V	19	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	19	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	36	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,32,37	DDR3 1.5V Rails	PS_S3CNTRL	S0



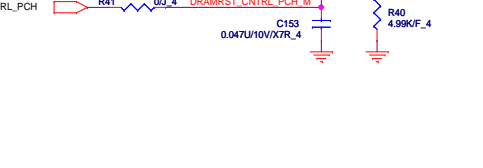
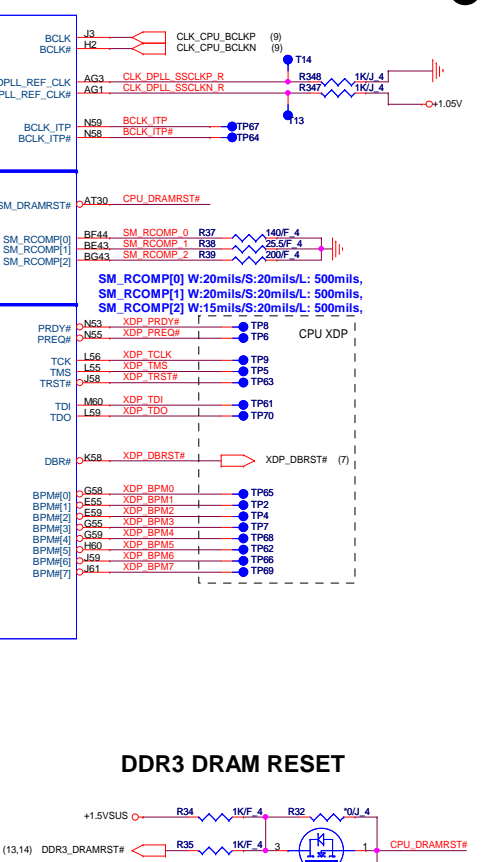
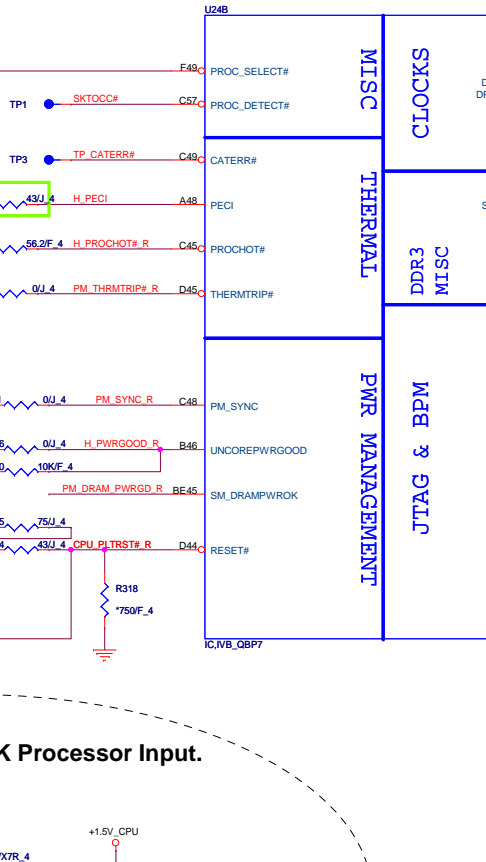
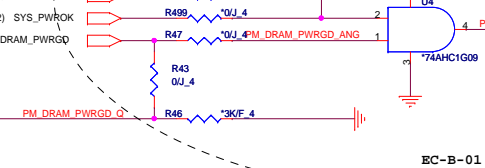
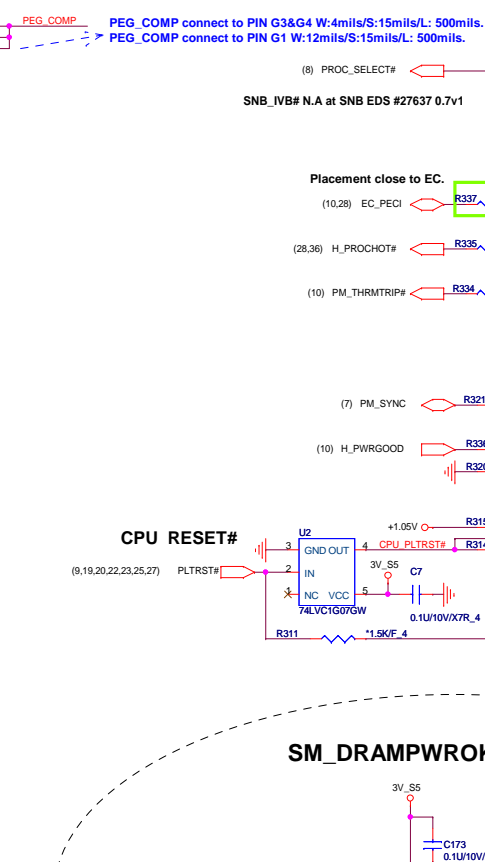
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PROJECT : LI2

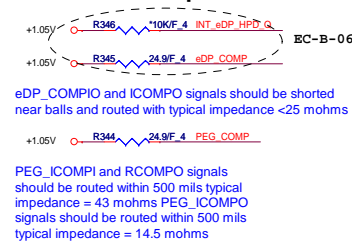
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	FRONTPAGE	1A
Date:	Wednesday, January 04, 2012	Sheet 2 of 49



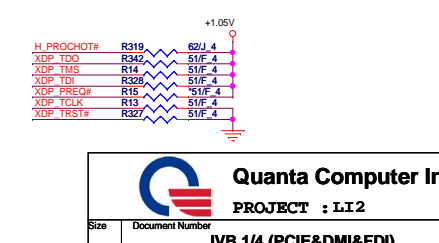
eDP_COMP connect to PIN AF3 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN AD2 W:12mils/S:15mils/L: 500mils.



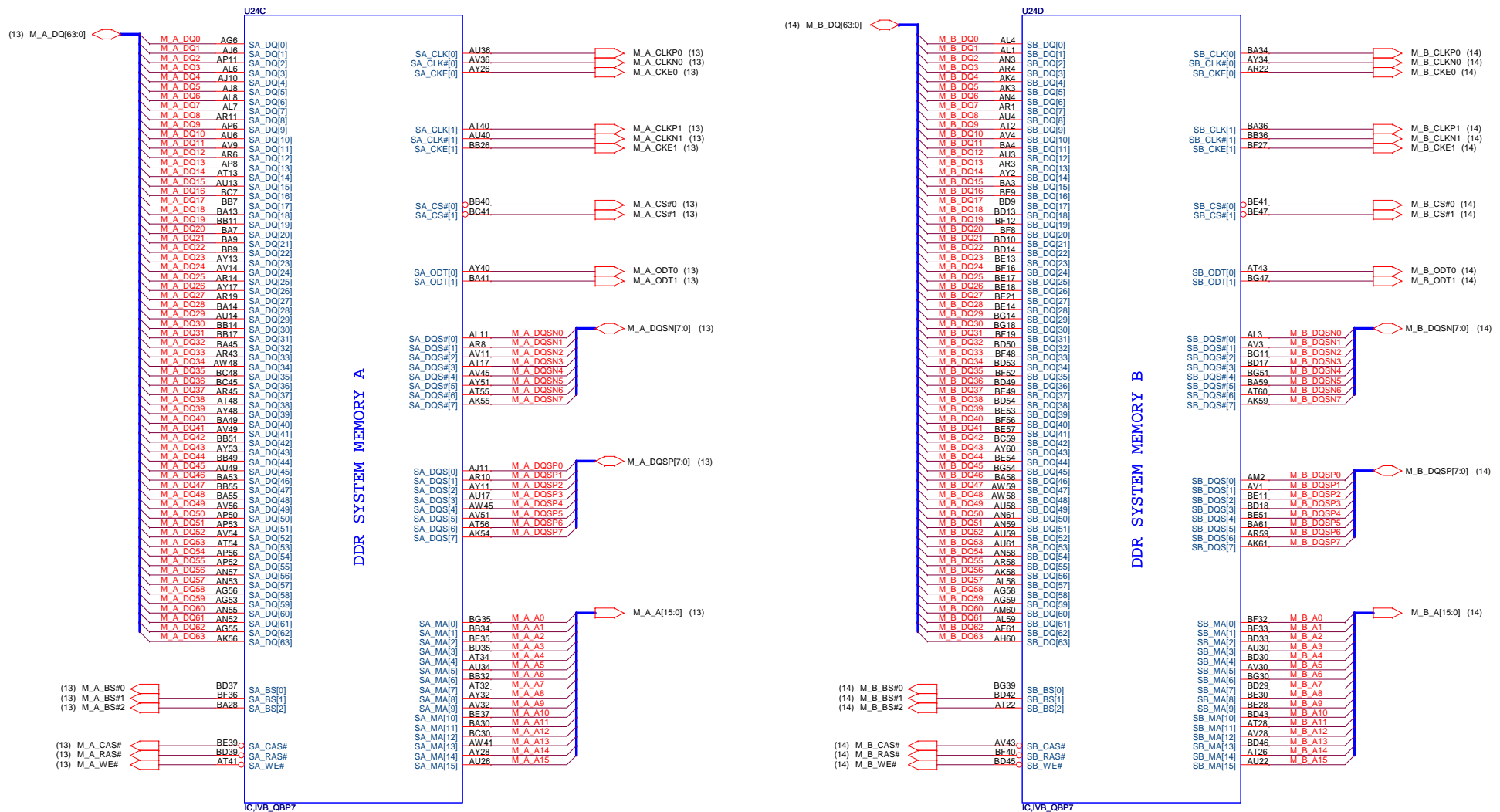
DP & PEG Compensation

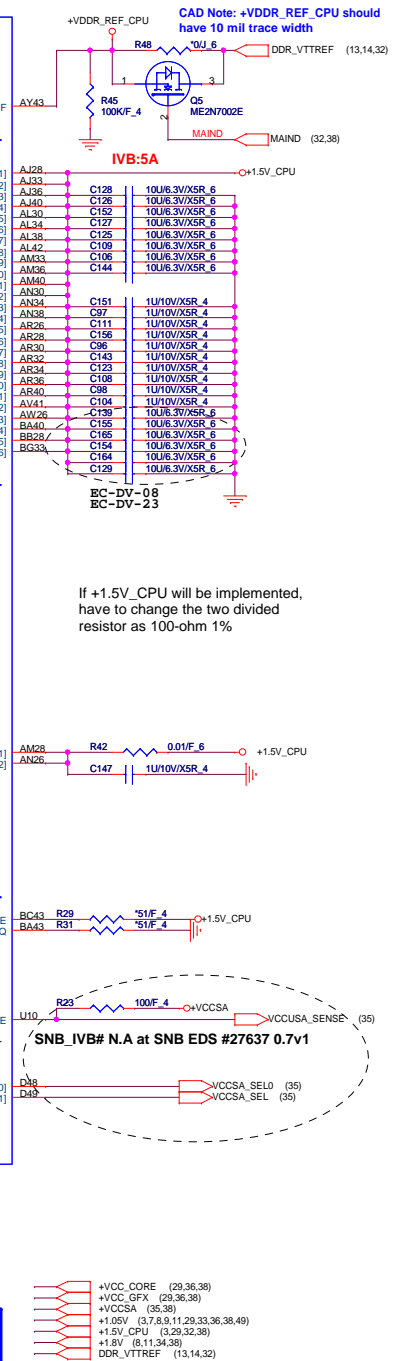
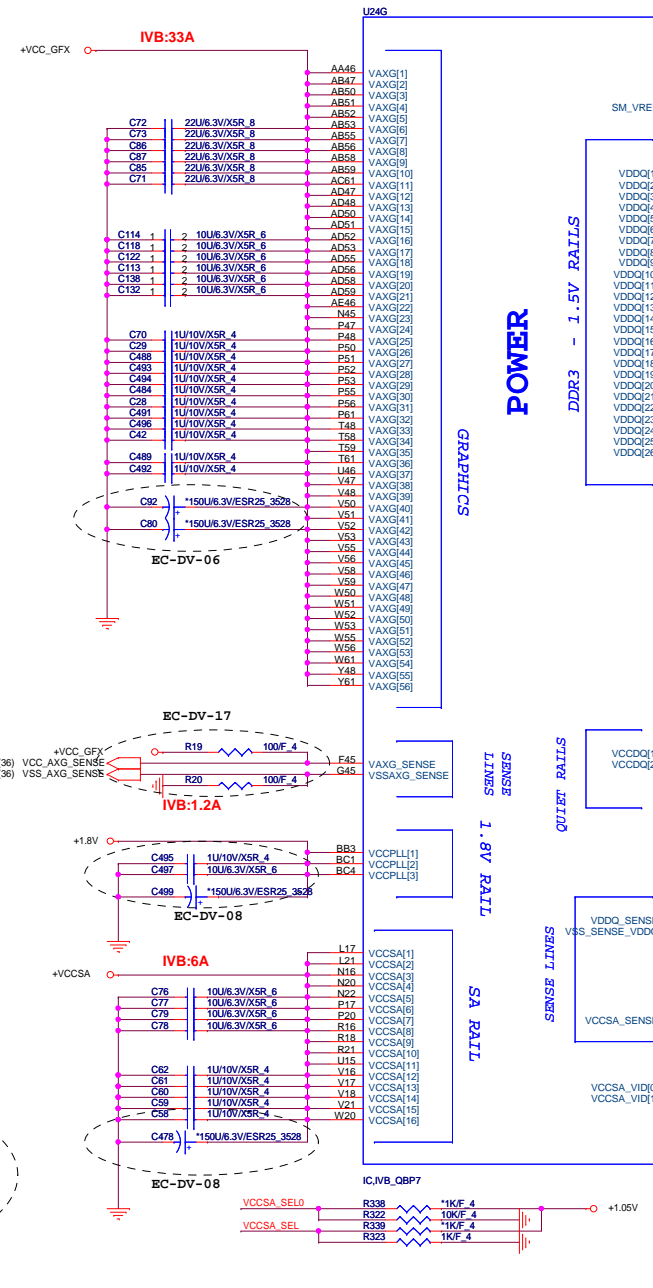


Processor pull-up (CPU)



IVY Bridge Processor (DDR3)





Place PU resistor close to CPU

+1.05V

R310 75J 4

H CPU_SVIDALRT#

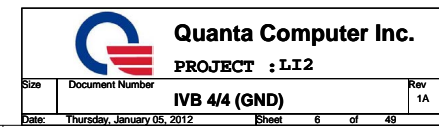
R332 43J 4

R309 0/J 4

VR_SVID_ALERT#

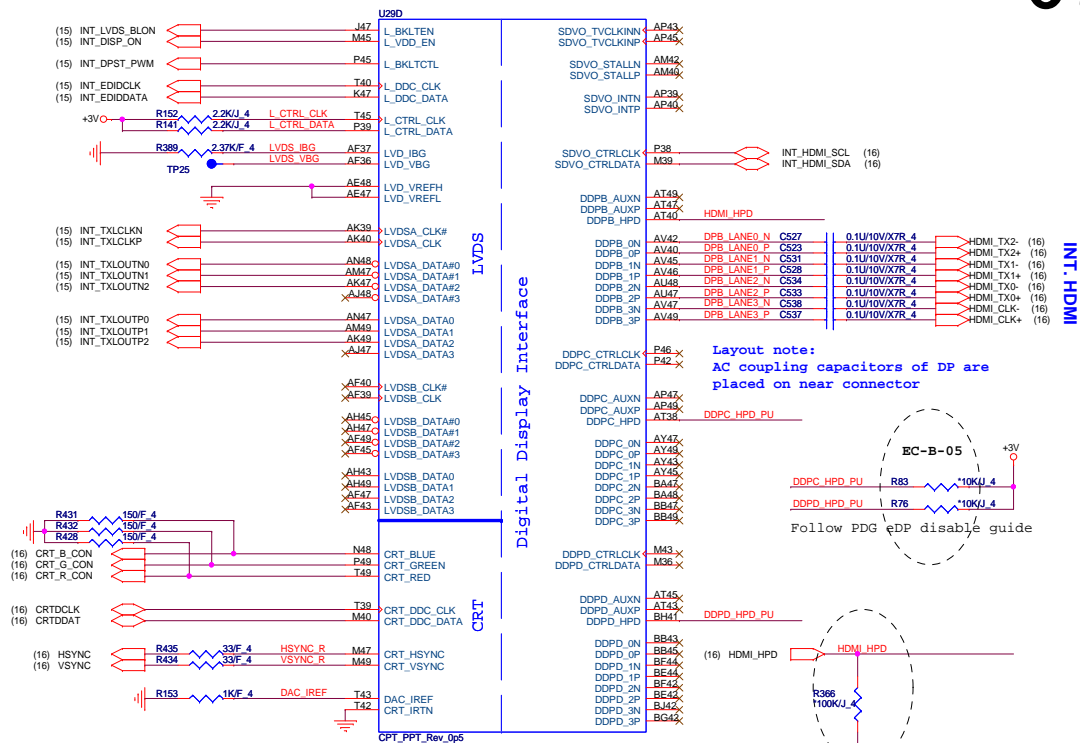
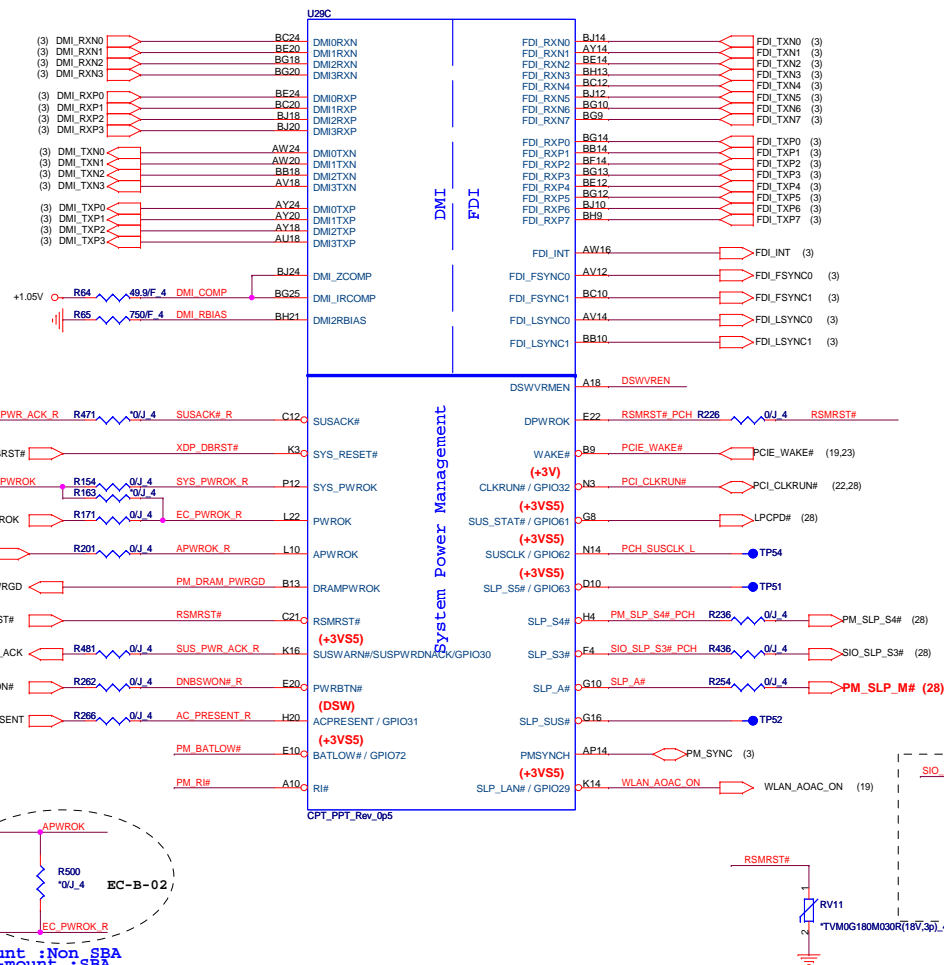
(36)

06



Cougar Point/Panther Point (DMI, FDI, PM)

Cougar Point/Panther Point (LVDS,DDI)



Layout note:
AC coupling capacitors of DP are
placed on near connector

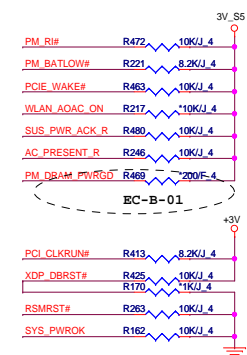
EC-B-05

DDPC HPD PU R83 *10KU_4 +3V

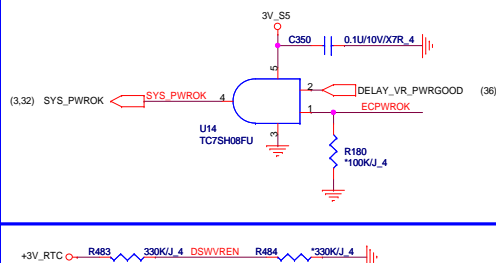
DDPD HPD PU R76 *10KU_4

Follow PDG eDP disable guide

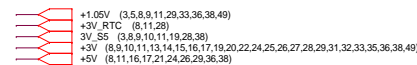
PCH Pull-high/low(CLG)



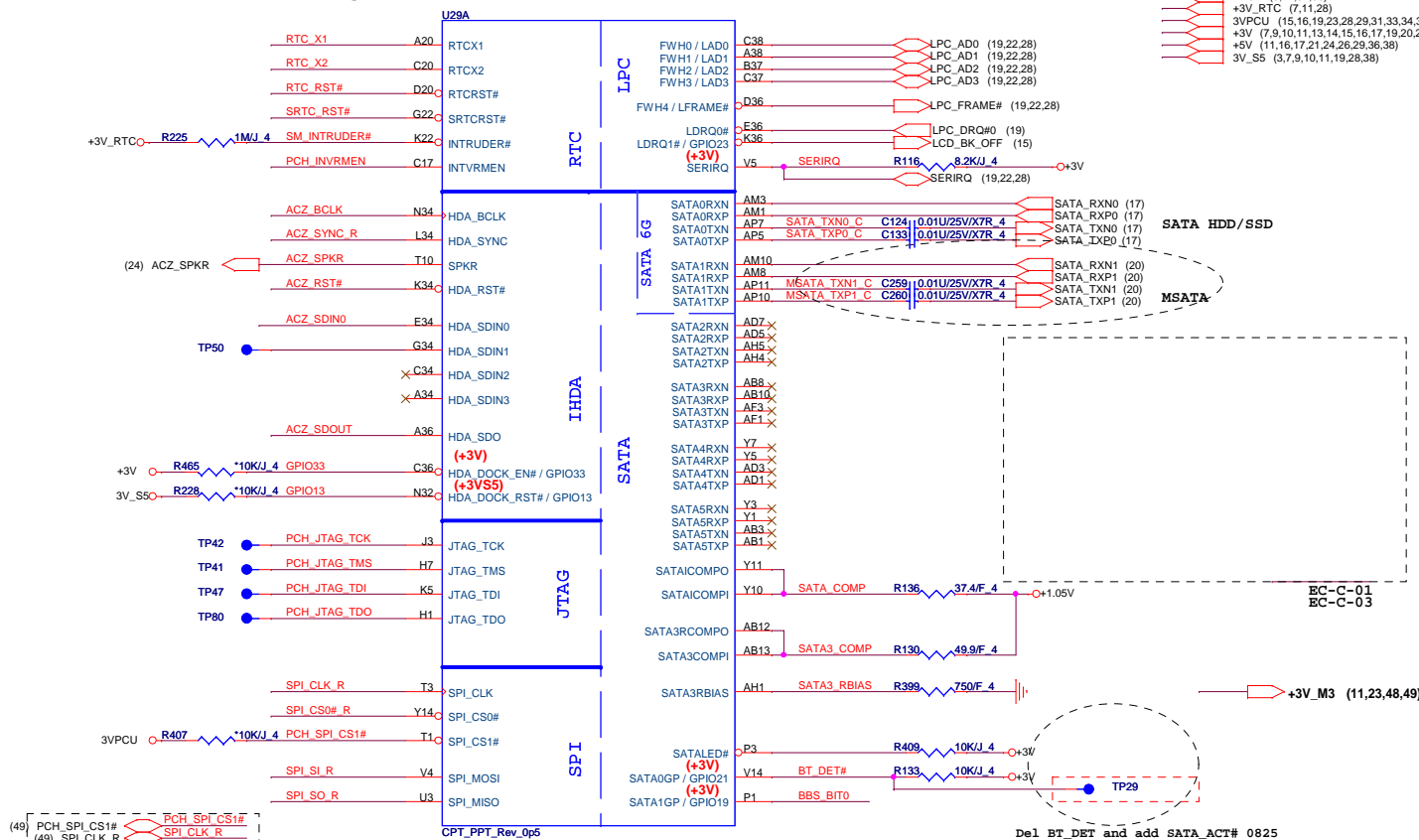
System PWR_OK(CLG)



On Die DSW VR Enable
High = Enable (Default) Low = Disable



Cougar Point/Panther Point (HDA,JTAG,SATA)

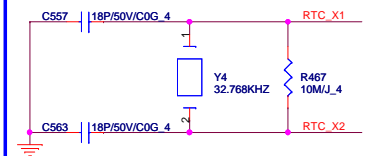


if default boot destination is SPI,
no external pull-up/-down resistors on the board are
necessary

PCH Strap Table

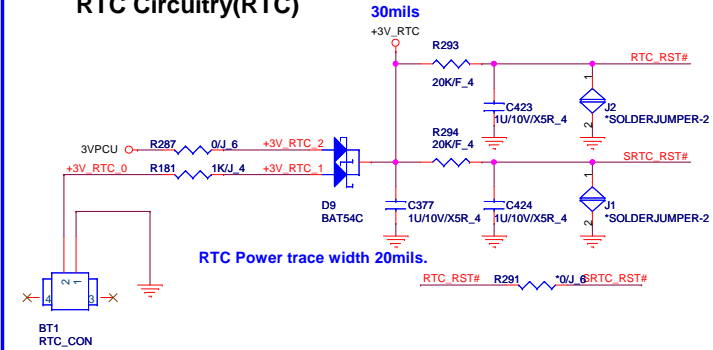
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella	No reboot mode setting	PWROK 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R143 *1KJ_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R459 *1KJ_4 R452 *10KJ_4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R468 330KJ_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R464 *1KJ_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	0 = effective(Default: weak pull down) 1 = Override	[Need external pull-down for LPC BIOS]
GPIO19	Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK	R410 *1KJ_4 R458 *1KJ_4 BBS_BIT0 (9)
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm	R382 22KJ_4 R384 1KJ_4 Q29 ME2N7002E R285 1M/F_6 ACZ_SYNC_R R250 1KJ_4
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	ACZ_SYNC_R R250 1KJ_4
GPIO15				(10) GPIO15 R433 1KJ_4 3V_S5
GPIO28	Different from Calpella	On-die PLL Voltage Regulator	RSMRST# 0 = Disable 1 = Enable (Default)	R166 *1KJ_4 PLL_ODVR_EN (10)
DSWVREN		0: disable 1: enable		

RTC Clock 32.768KHz



08

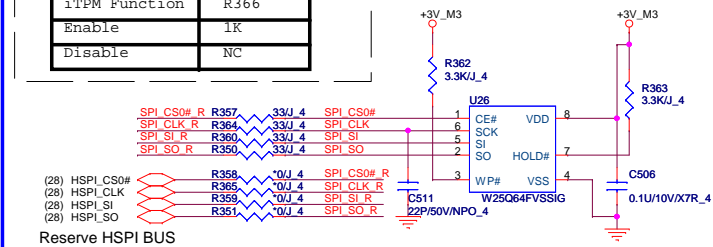
RTC Circuitry(RTC)



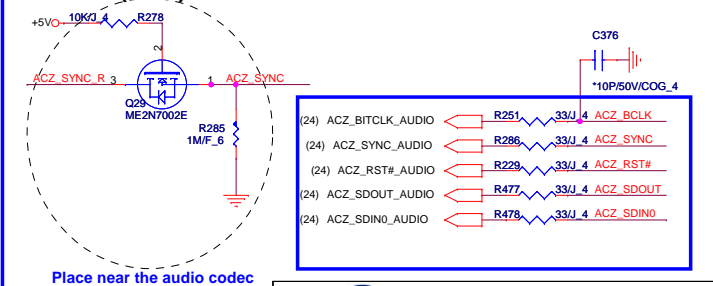
iTPM ENABLE/DISABLE

iTPM Function	R366
Enable	1K
Disable	NC

For PCH
32Mbit (4M Byte), SPI



HDA Bus(CLG)

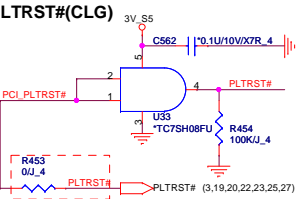
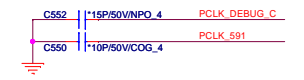
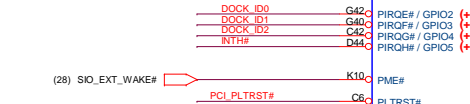
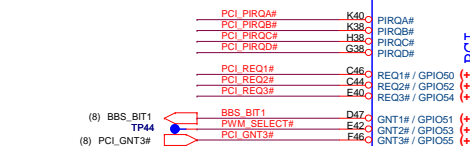
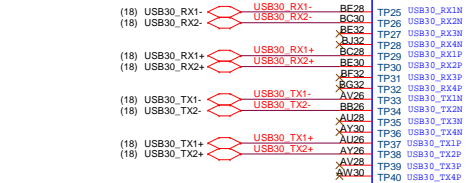
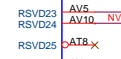
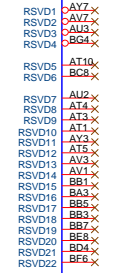
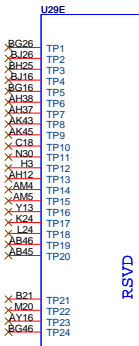
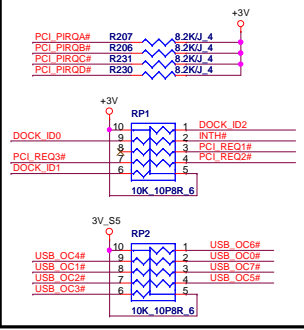


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PROJECT : LI2

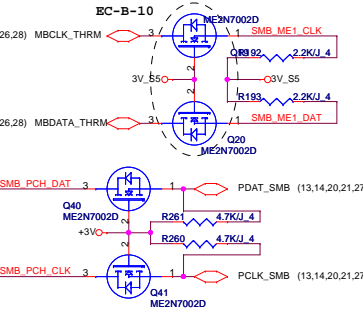
Cougar Point/Panther Point (PCI, USB, NVRAM)

Cougar Point/Panther Point((PCI-E,SMBUS,CLK)

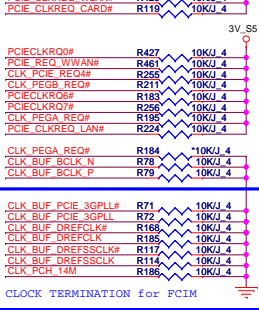
PCI/USBOC# Pull-up(CLG)



SMBus/Pull-up(CLG)



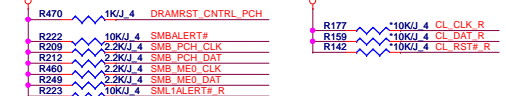
CLK_REQ/Strap Pin(CLG)



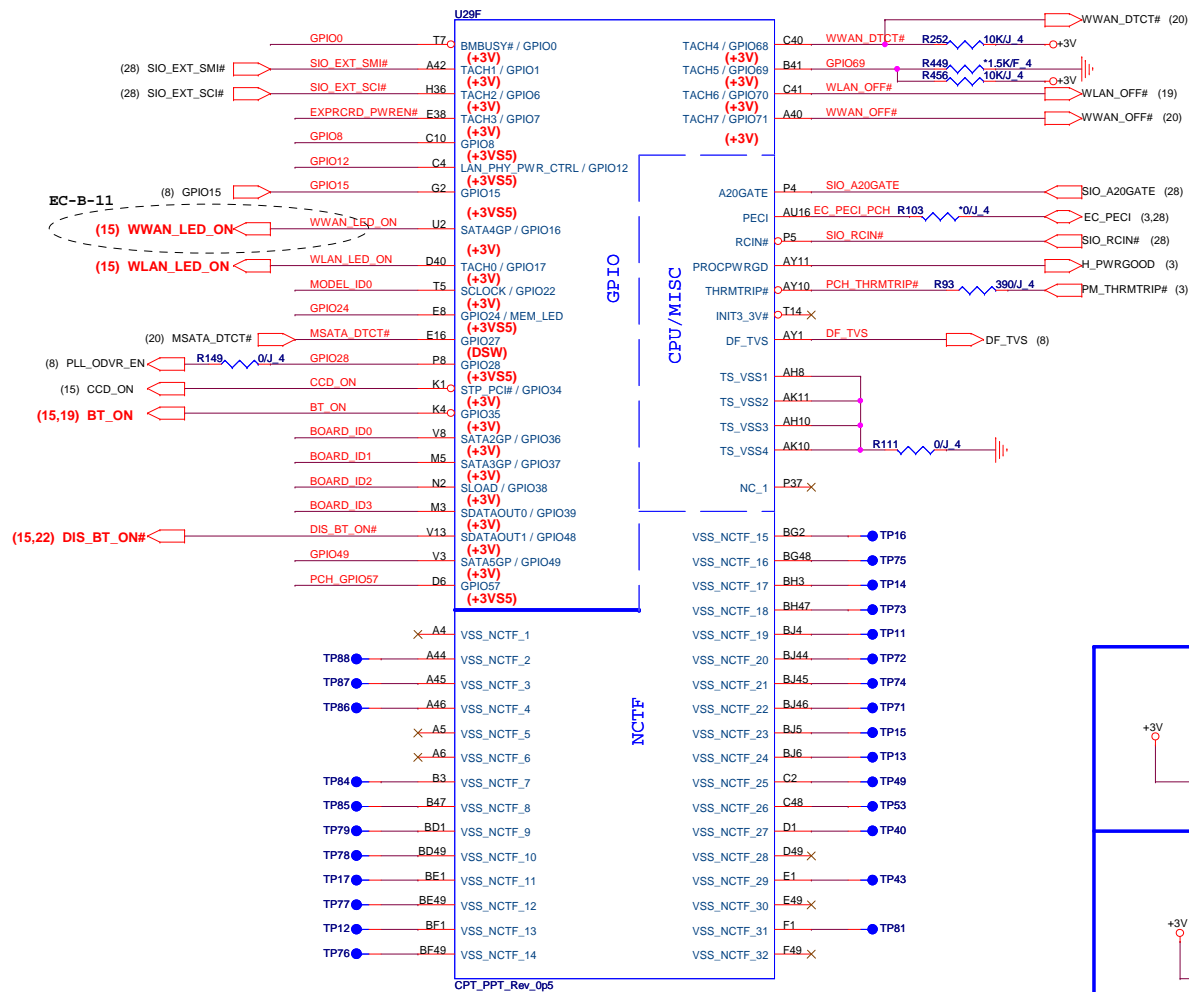
PCIE Clock

Layout note:
PCIE_CLKREQ_LAN# layout adjacent
to CLK_PEGA_REQ#

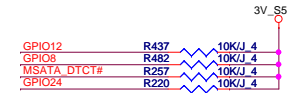
SMBus/Pull-up(CLG)



Cougar Point/Panther Point(GPIO,VSS_NCTF,RSVD)

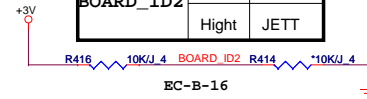


GPIO Pull-up/Pull-down(CLG)



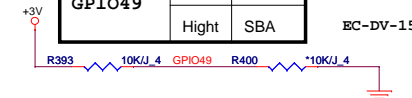
PROJECT ID SETTING

BOARD_ID2	Low	Dutton
	High	JETT



SBA SETTING

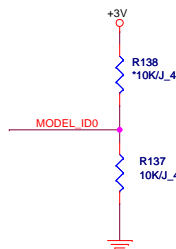
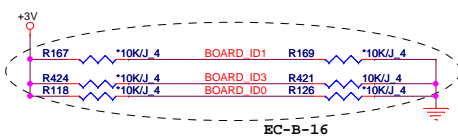
GPIO49	Low	N.A
	High	SBA



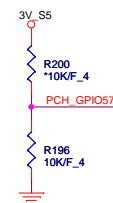
BOARD ID SETTING

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0

Model ID	MODEL_ID0
INTEL	0
AMD	1



TPM physical presence
PCH_GPIO57 Low: Default

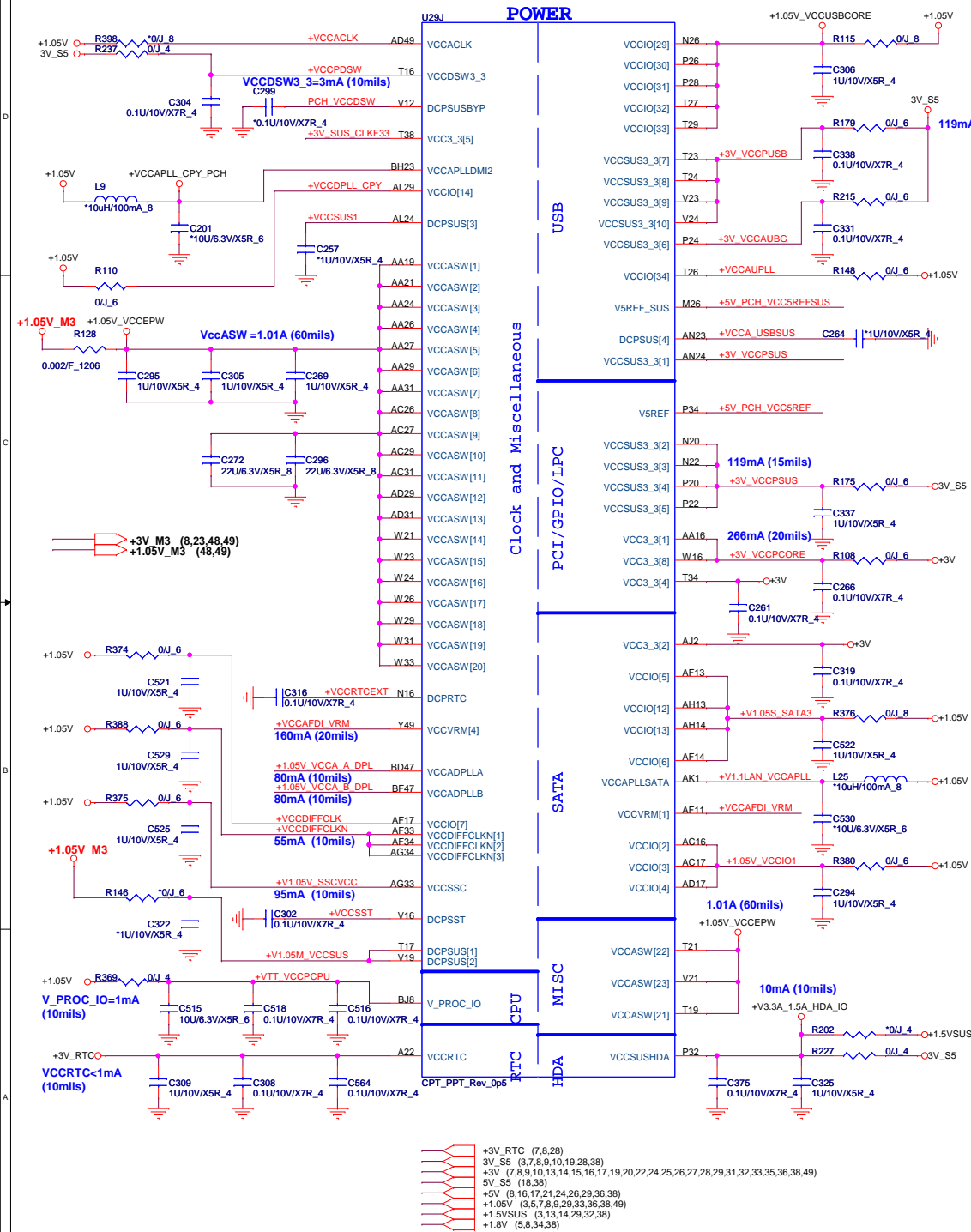


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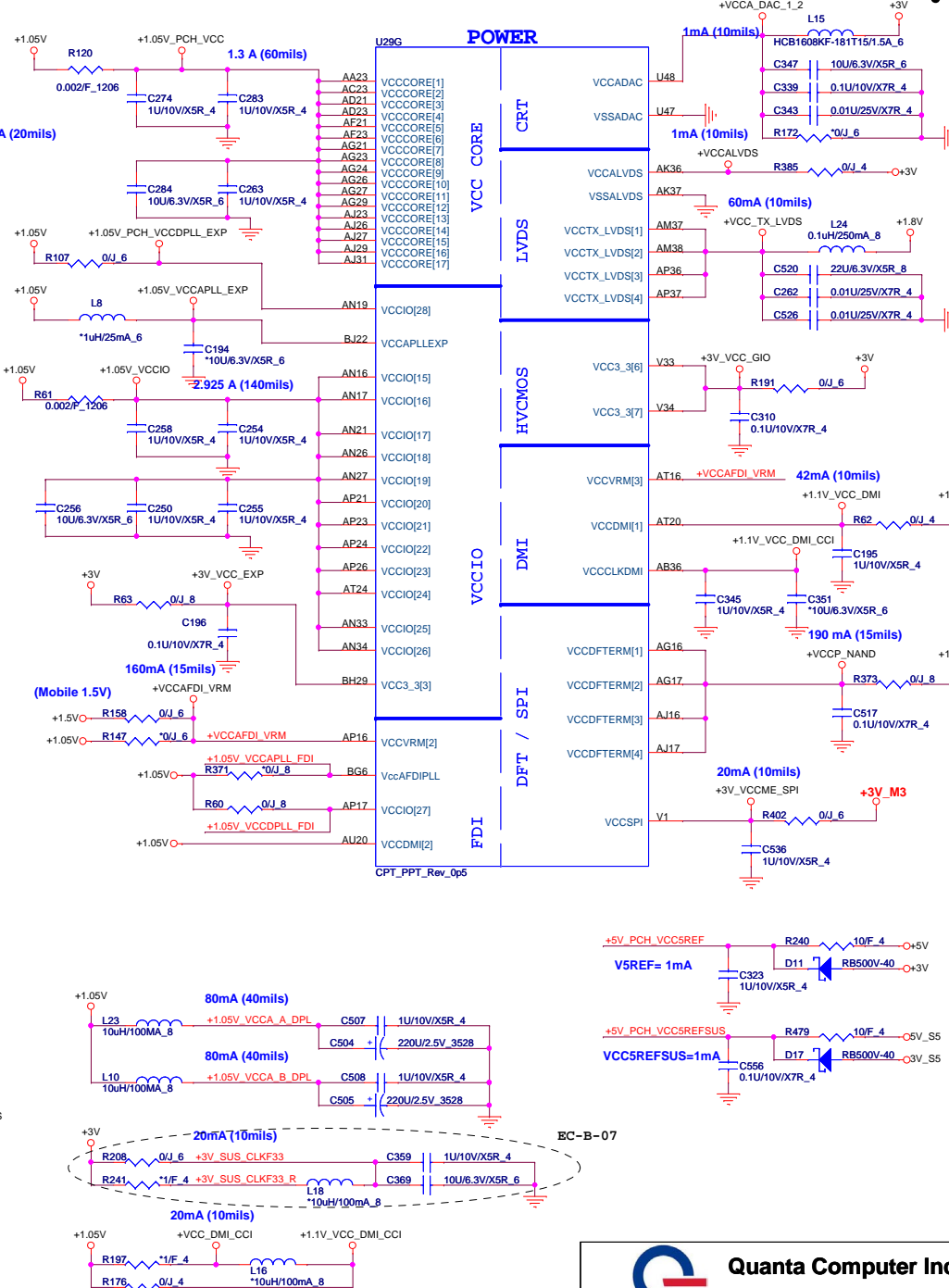
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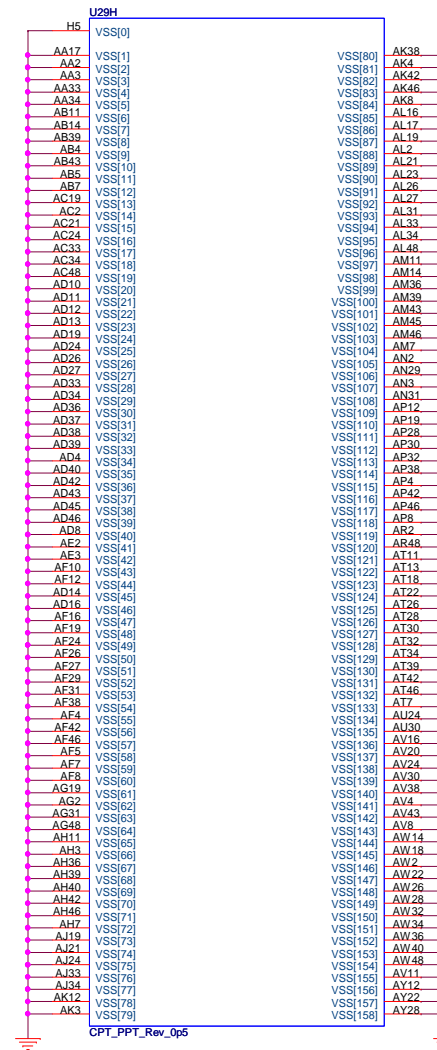
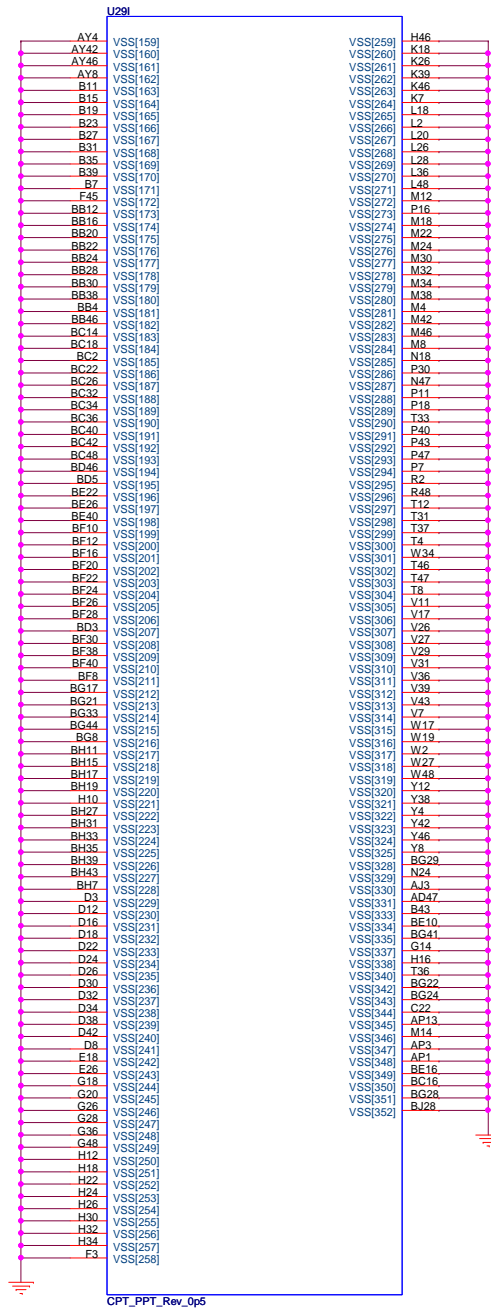
PCH 4/6 (GPIO/MISC)

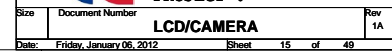
Cougar Point/Panther Point (POWER)

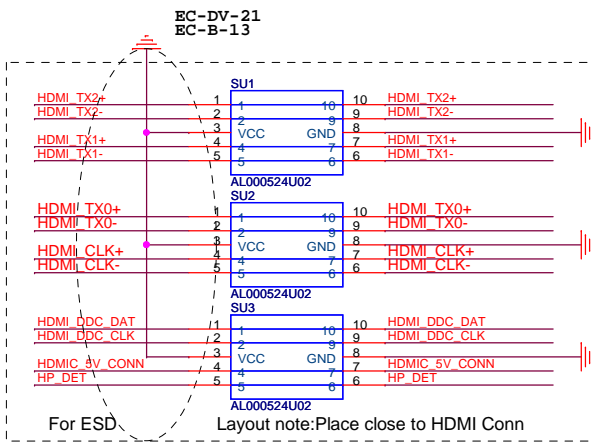
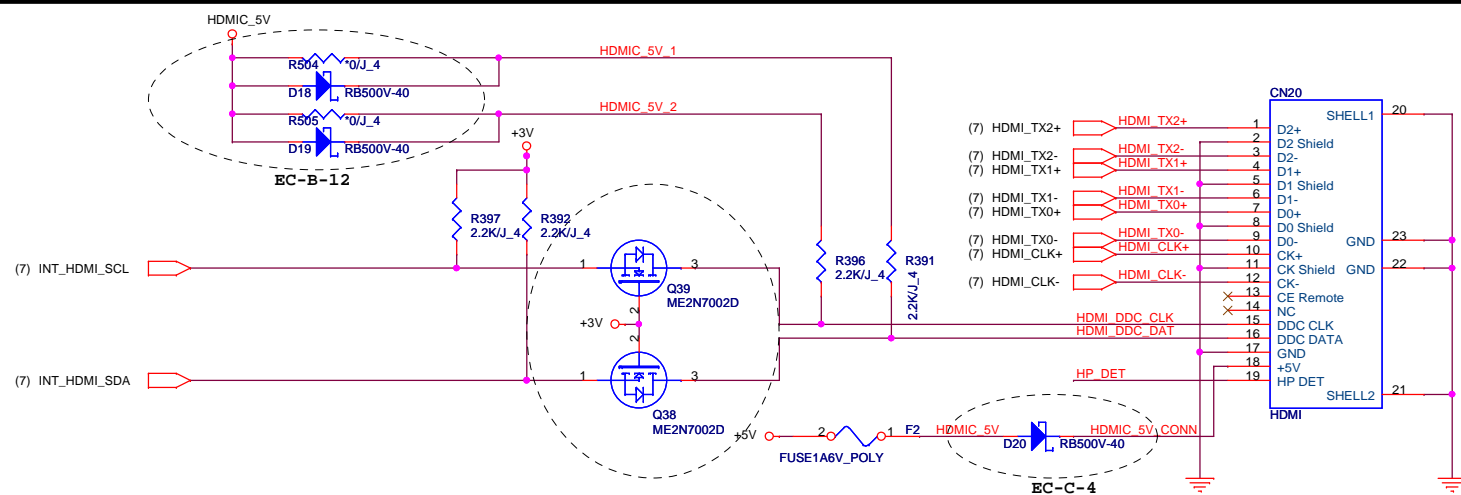
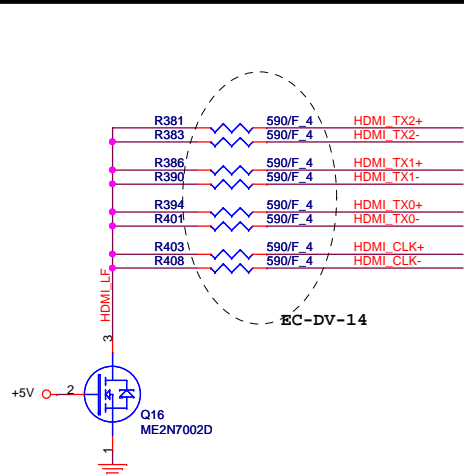
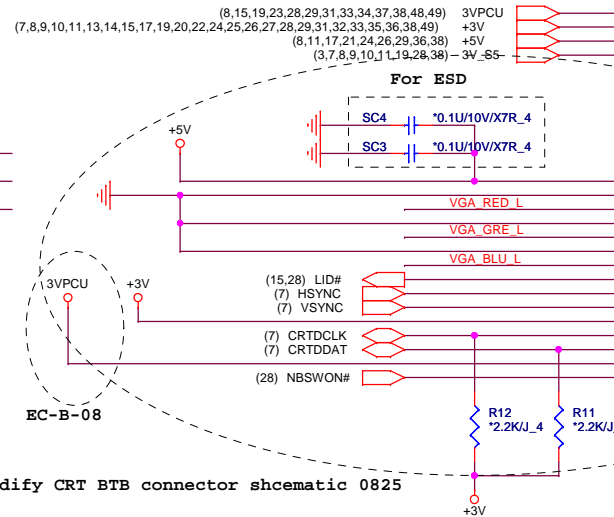
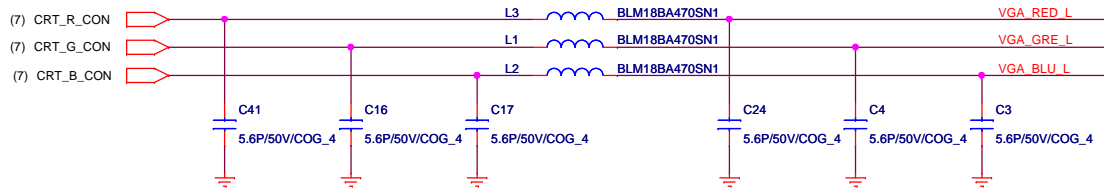


Cougar Point/Panther Point (POWER)

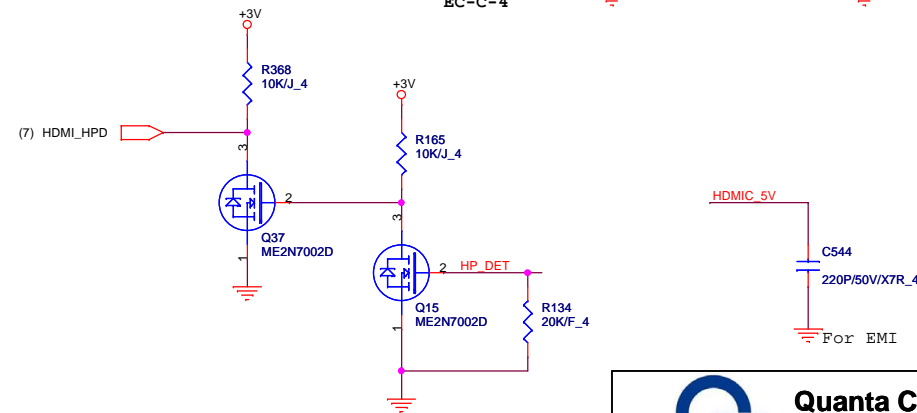
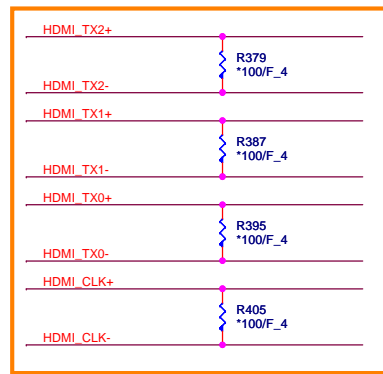








EMI reserve for HDMI



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PROJECT : LI2

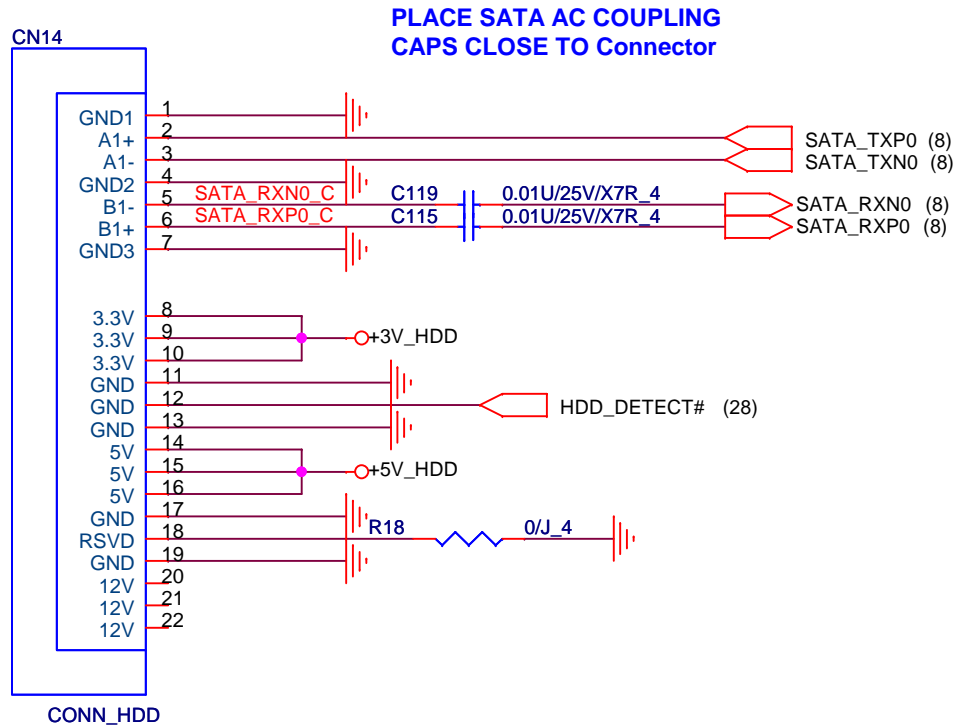
Size Document Number

CRT/HDMI CONN

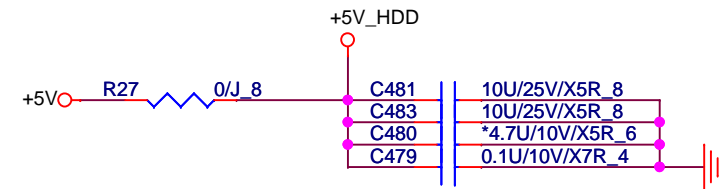
Date: Thursday, January 05, 2012 Sheet 16 of 49

Rev 1A

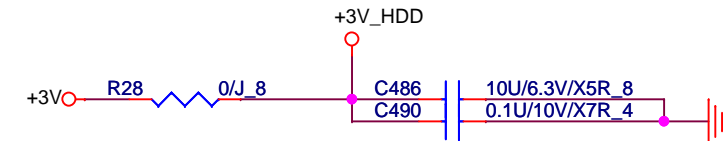
+3V (7,8,9,10,11,13,14,15,16,19,20,22,24,25,26,27,28,29,31,32,33,35,36,38,49)
+5V (8,11,16,21,24,26,29,36,38)



DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



Quanta Computer Inc.

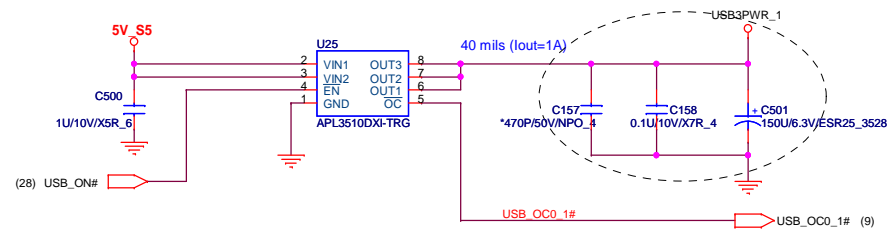
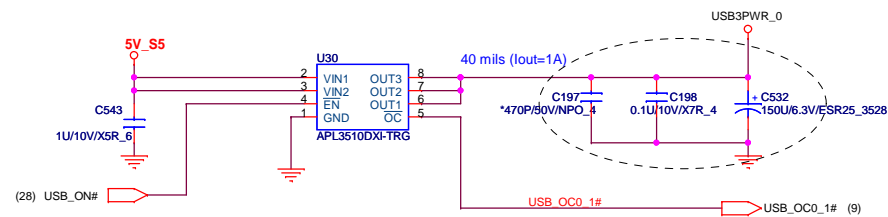
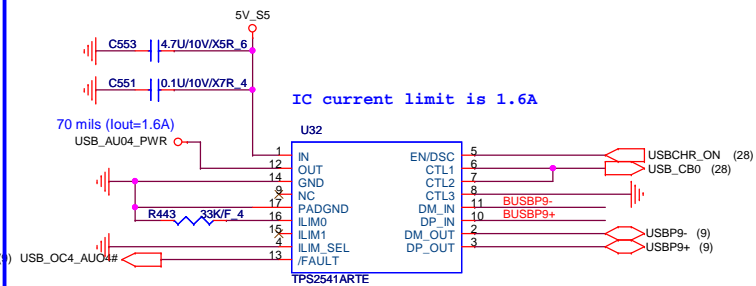
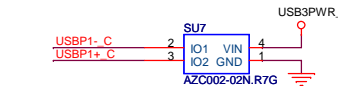
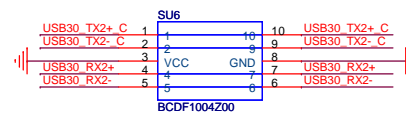
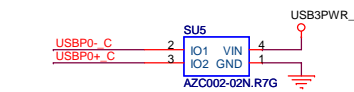
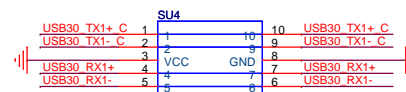
PROJECT : LI2

Size	Document Number	Rev
	SATA	1A
Date:	Thursday, January 05, 2012	Sheet 17 of 49

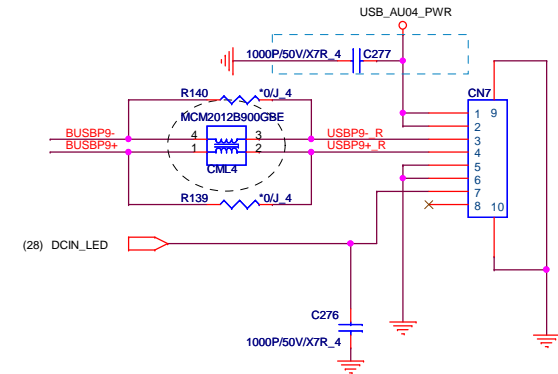
TPS2541 table

CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

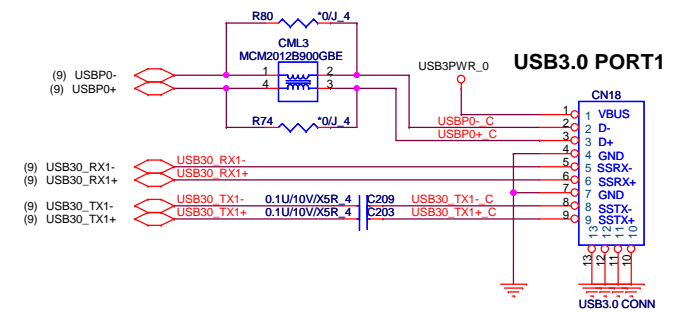
Table 3 – TPS2541 Control Truth Table

EC-B-13
EC-DV-05

USB BTB CONN

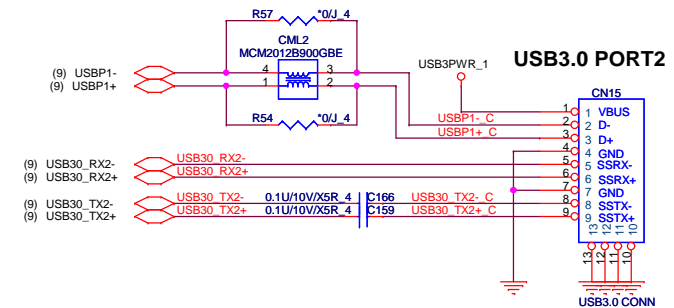


USB3.0 PORT1



SUY USB3.0: DFHS09FR063

USB3.0 PORT2



SUY USB3.0: DFHS09FR063



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PROJECT : LI2

Size Document Number

CONN USB x 3

Rev 1A

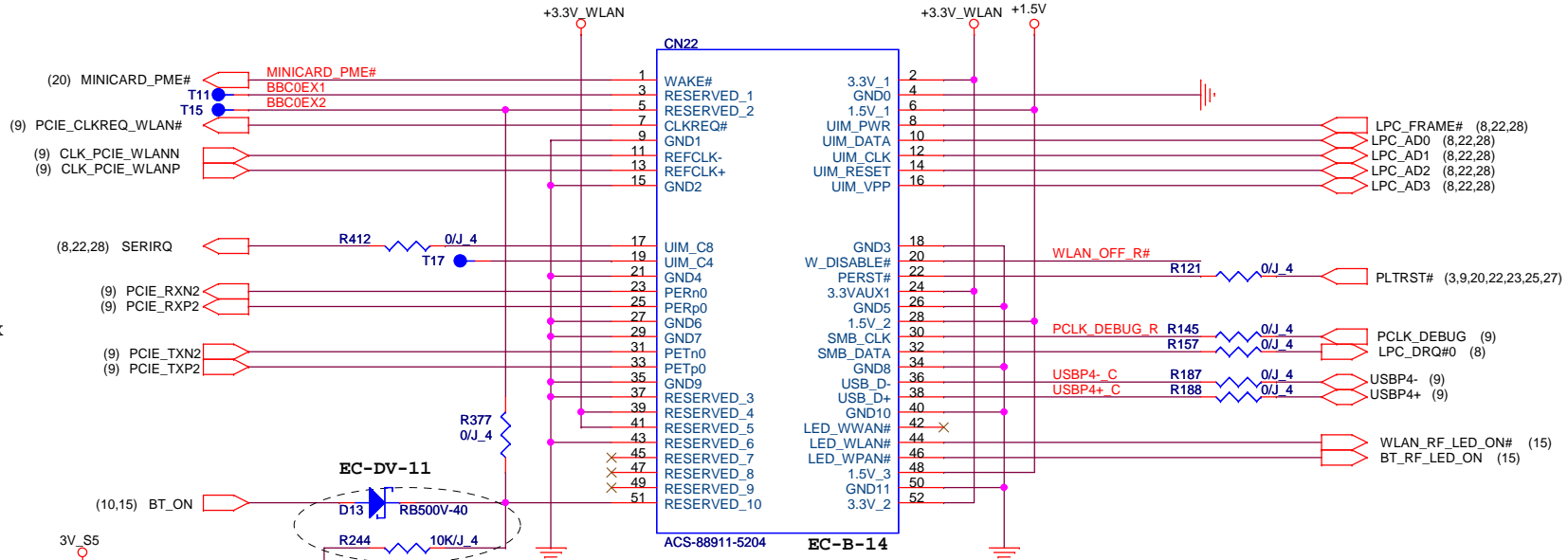
Date: Friday, January 06, 2012

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MiniCard WLAN connector

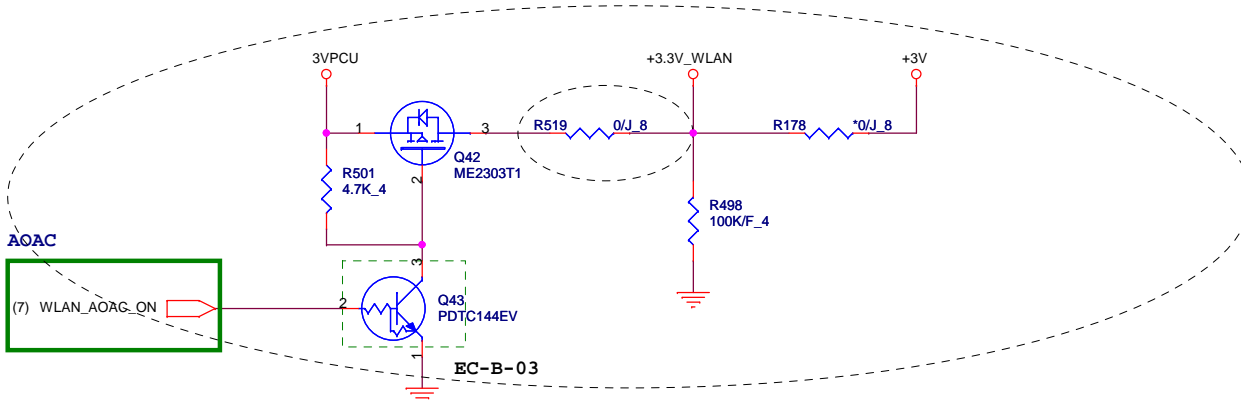
+3V (7,8,9,10,11,13,14,15,16,17,20,22,24,25,26,27,28,29,31,32,33,35,36,38,49)
 +1.5V (11,20,32,38)
 3V_S5 (3,7,8,9,10,11,28,38)

19

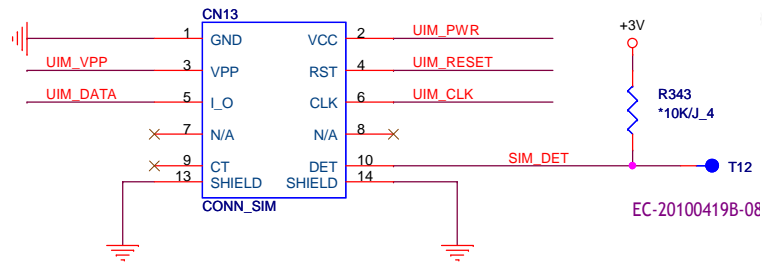


PCI-Express TX and RX direct to connector

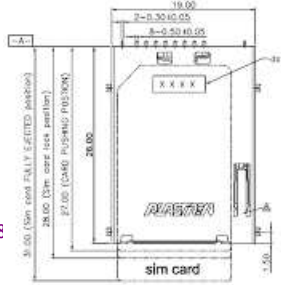
Place caps close to connector. close to CN22



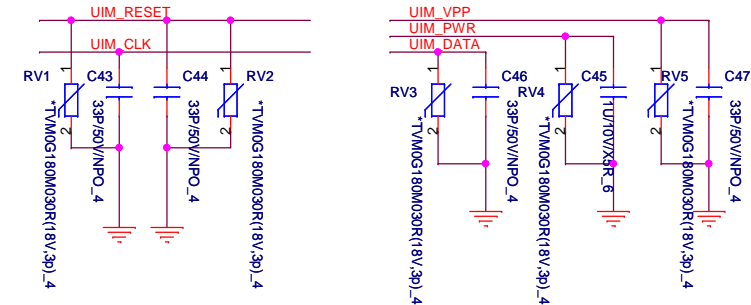
SIM Card CONN



Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible

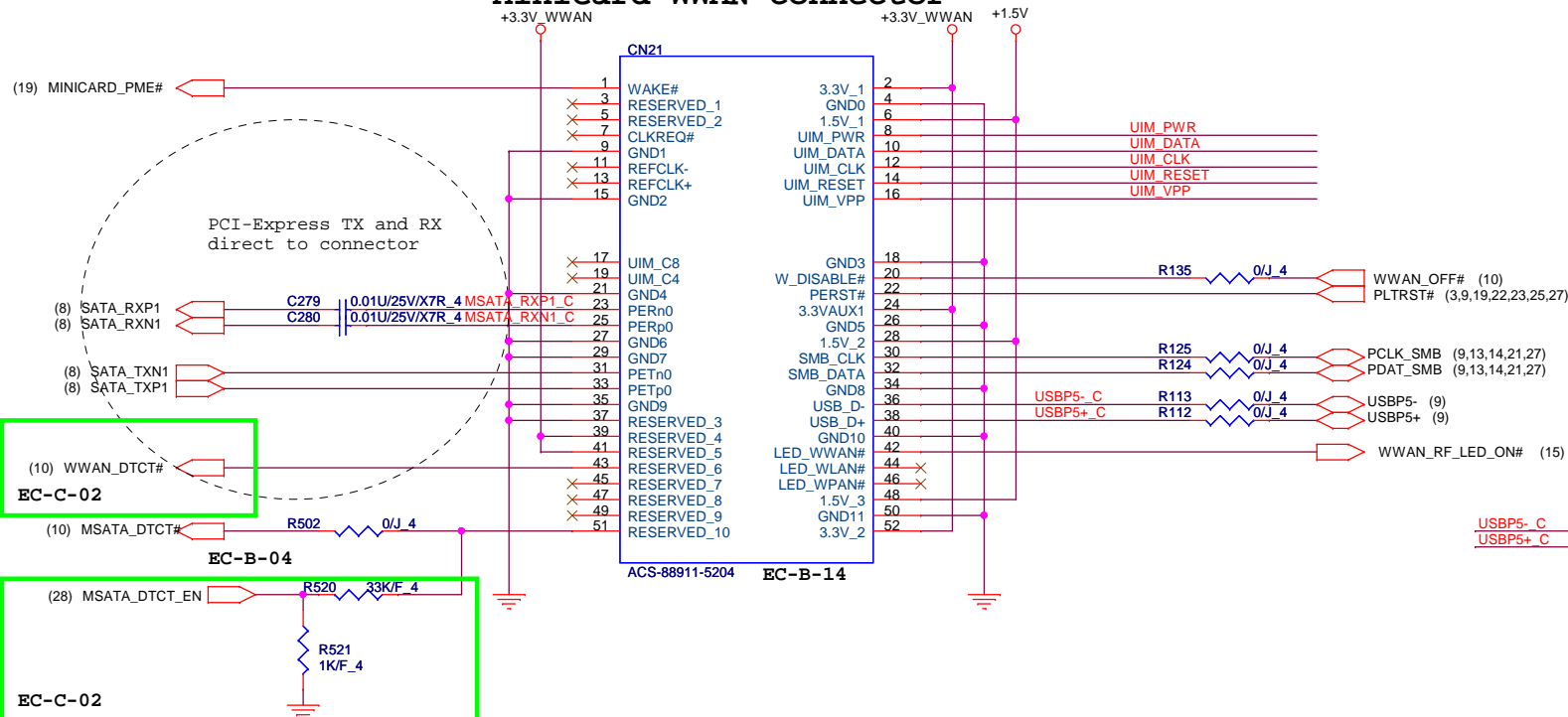


+3V (7,8,9,10,11,13,14,15,16,17,19,22,24,25,26,27,28,29,31,32,33,35,36,38,49)
+1.5V (11,19,32,38)



EC-DV-22

MiniCard WWAN connector



PCI-Express TX and RX direct to connector

Place caps close to connector.

close to CN22



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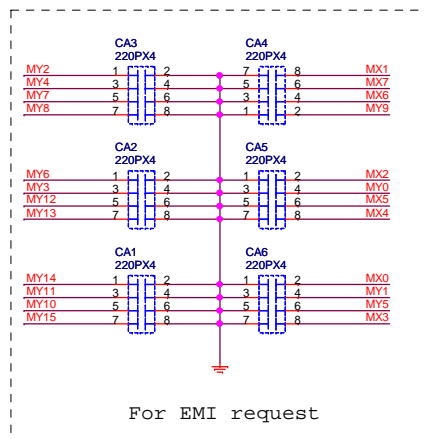
PROJECT : LI2

WWAN+MSATA

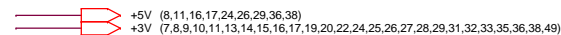
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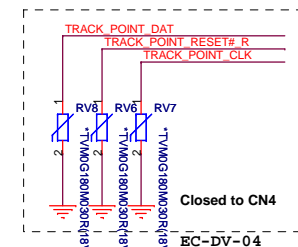
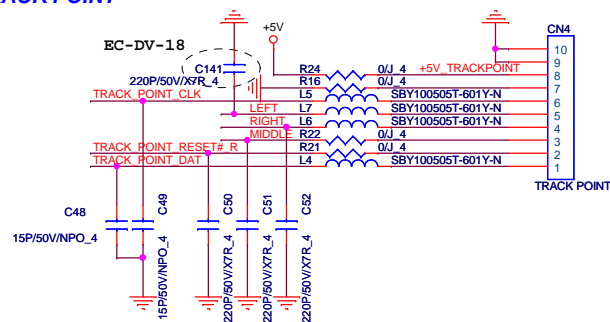


For EMI request

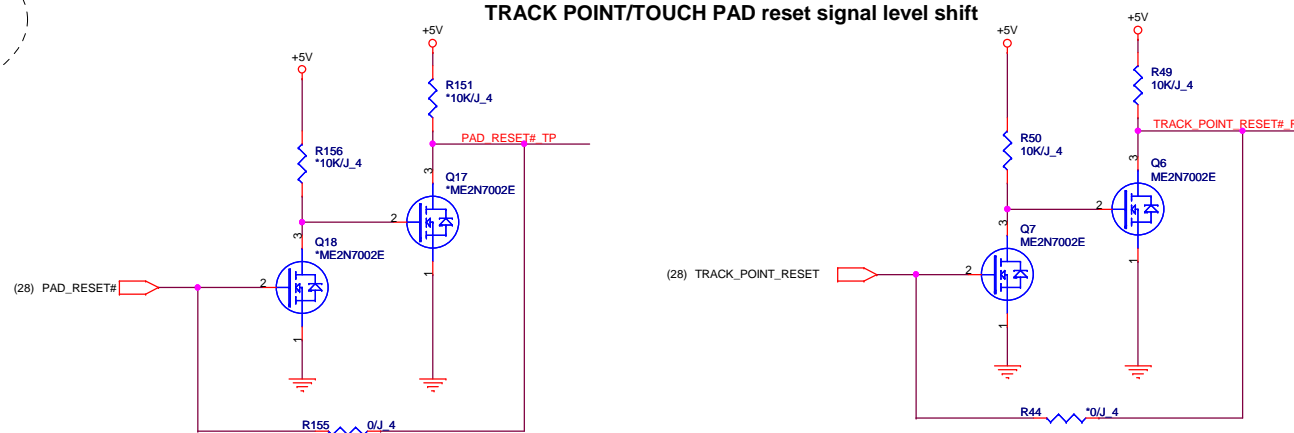


Remove fringer printer schcematic

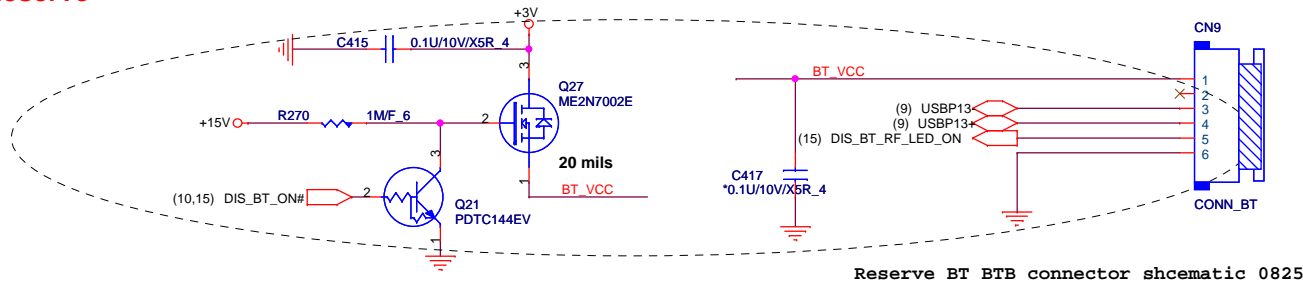
TRACK POINT



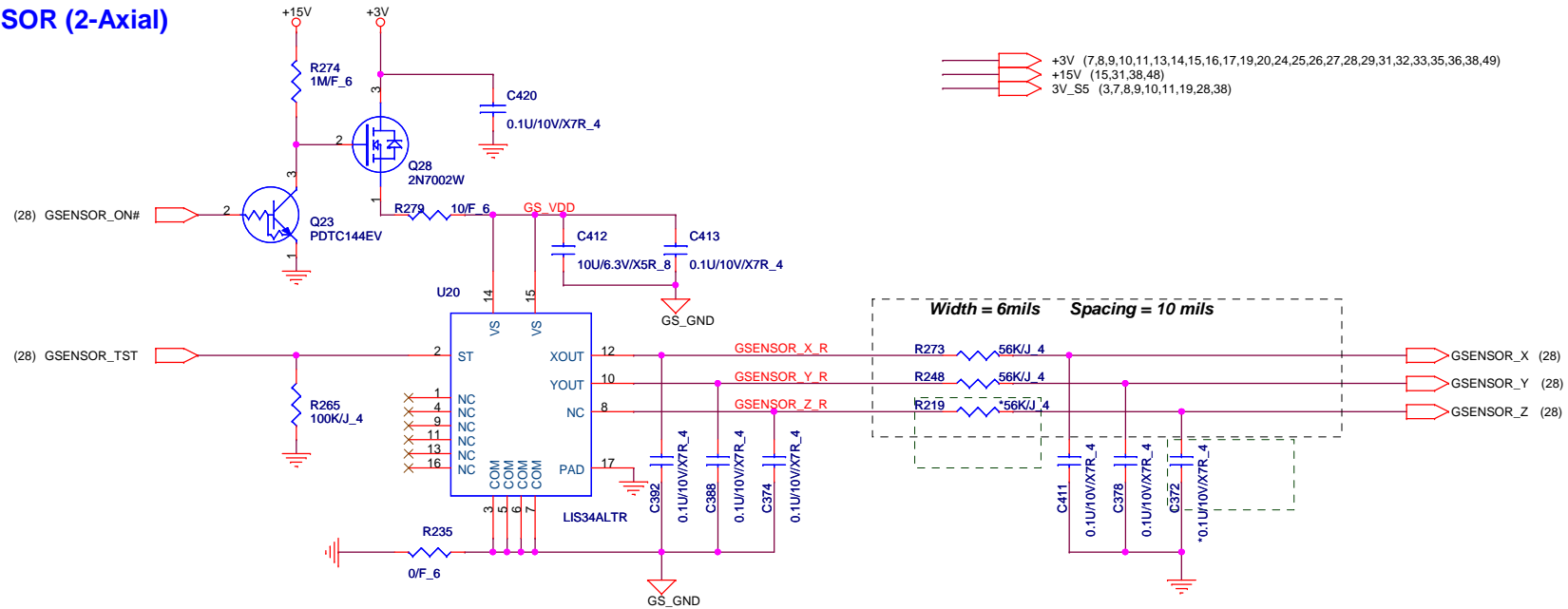
TRACK POINT/TOUCH PAD reset signal level shift



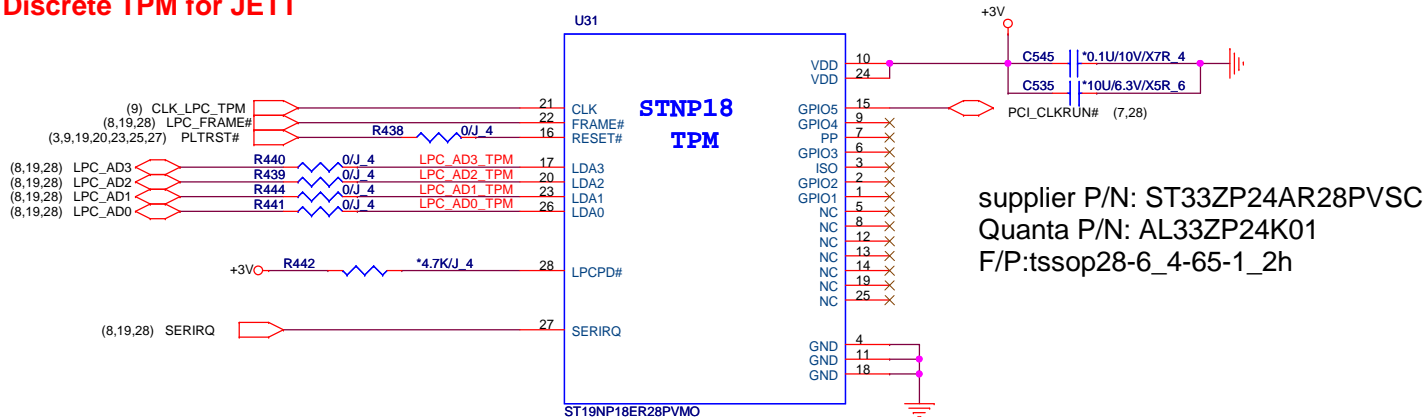
BLUETOOTH Reserve



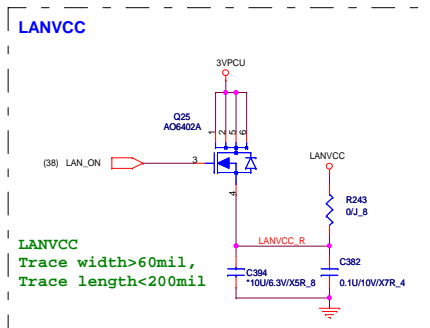
G-SENSOR (2-Axial)



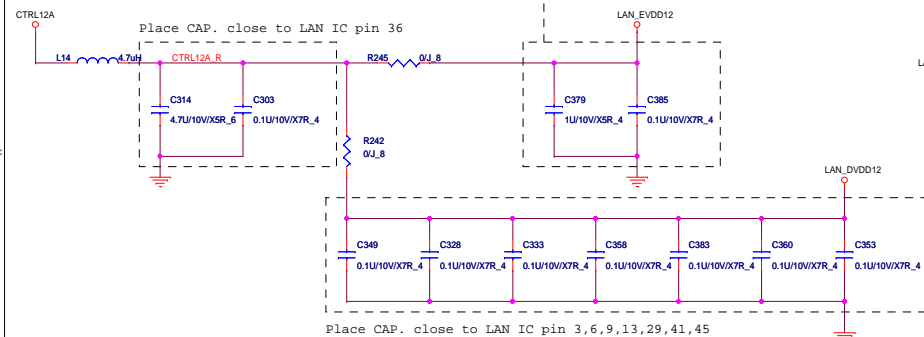
Discrete TPM for JETT



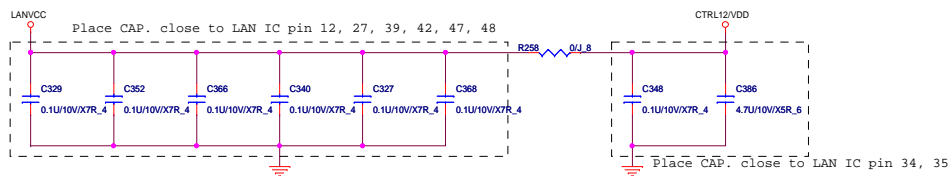
LAN: RTL8111F-CG



Place CAP. close to LAN IC pin 21



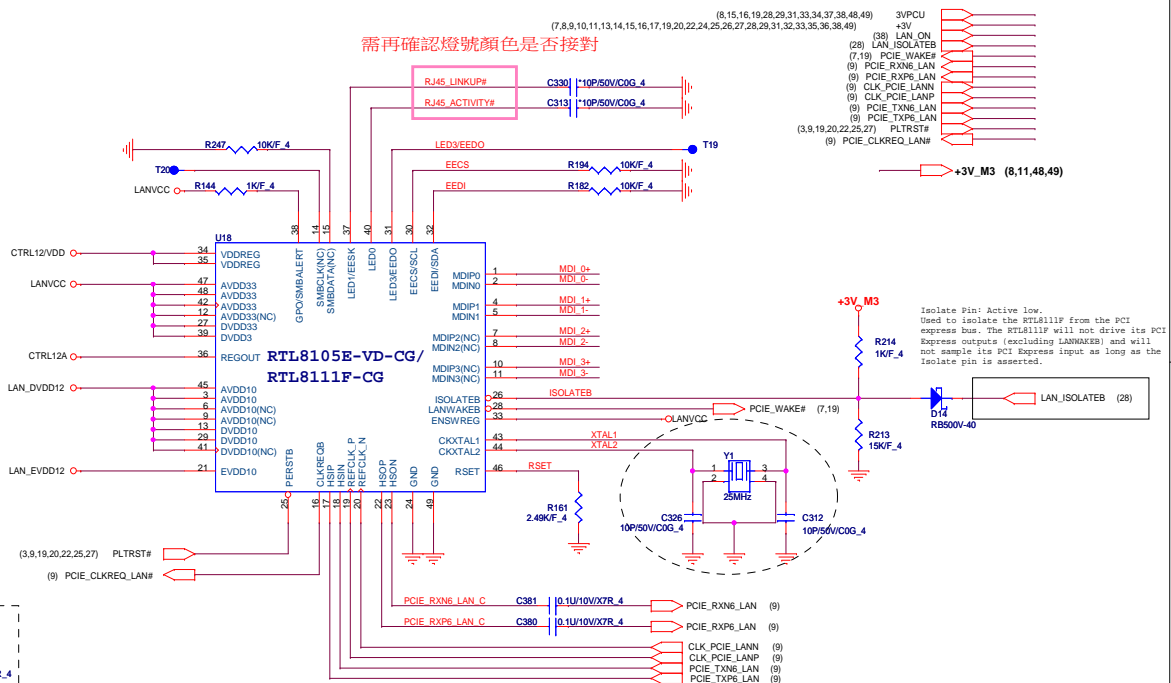
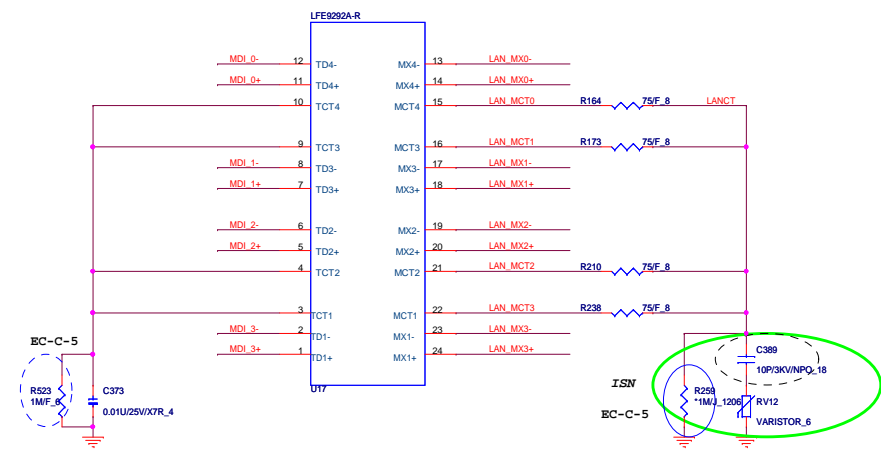
Place CAP. close to LAN IC pin 3,6,9,13,29,41,45



Place CAP. close to LAN IC pin 34, 35

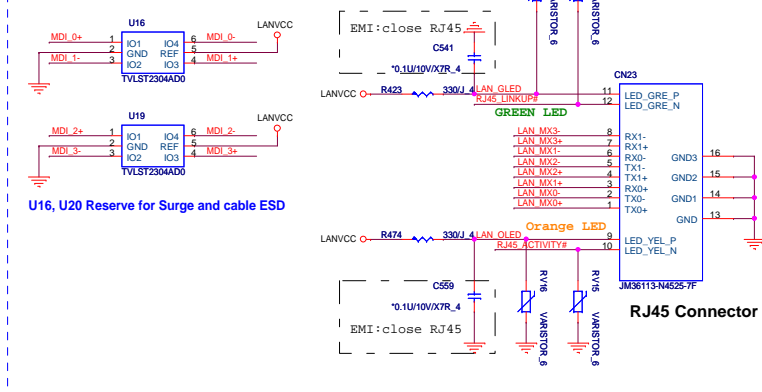
Transformer

Layout: All termination signal should have 20 mil trace



Isolate Pin: Active low.
Used to isolate the RTL8111F from the PCI
express bus. The RTL8111F will not drive its PCI
Express outputs (excluding LANWAKES) and will
not sample its PCI Express input as long as the
Isolate pin is asserted.

RJ45 Connector

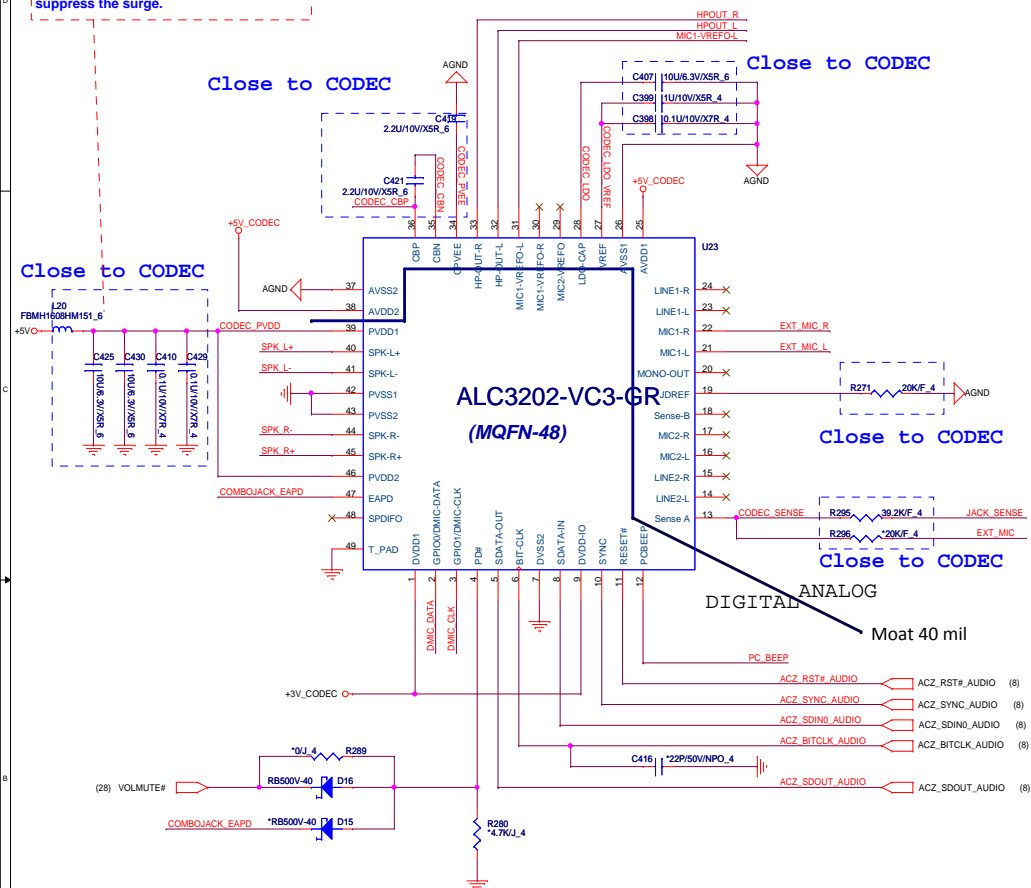


U16, U20 Reserve for Surge and cable ESD

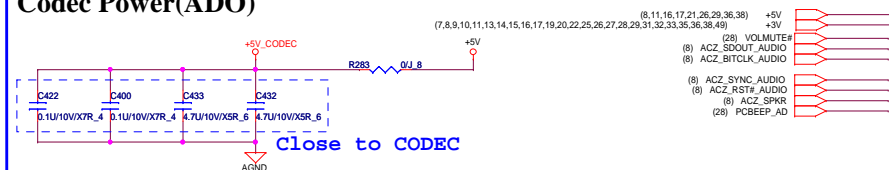
RJ45 Connector

CODEC(ADO)

- Surges of PVDD >TV duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.



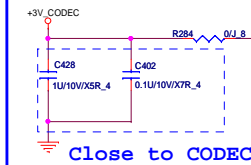
Codec Power(ADO)



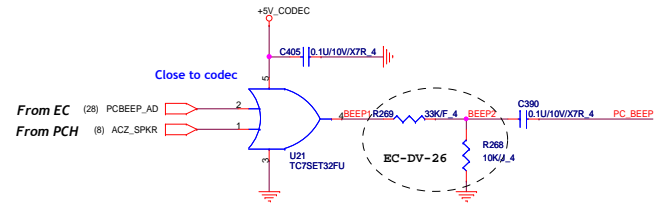
24

HDA Power(ADO)

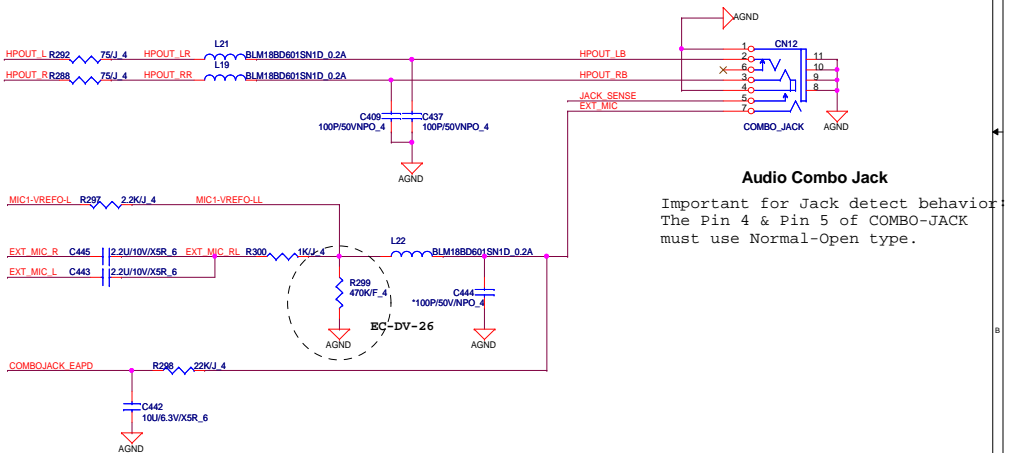
*Intel HDA Either +1.5V_S5 or +3V_S5



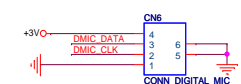
PC BEEP



External MIC/Headphone Combo

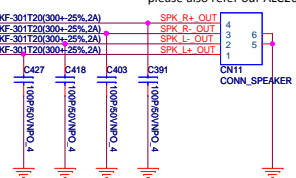
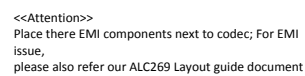


INT Digital MIC

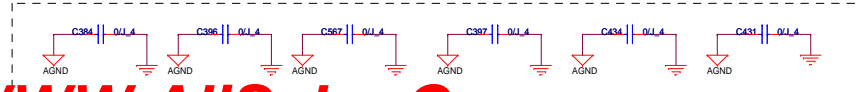


Internal Speaker

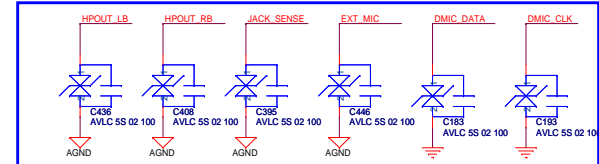
SPK L+ R+ trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils



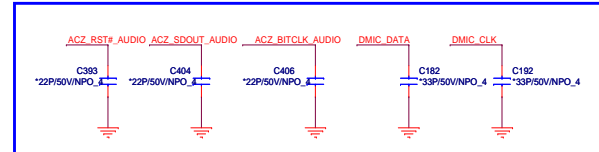
EMI Reserve



ESD Reserve

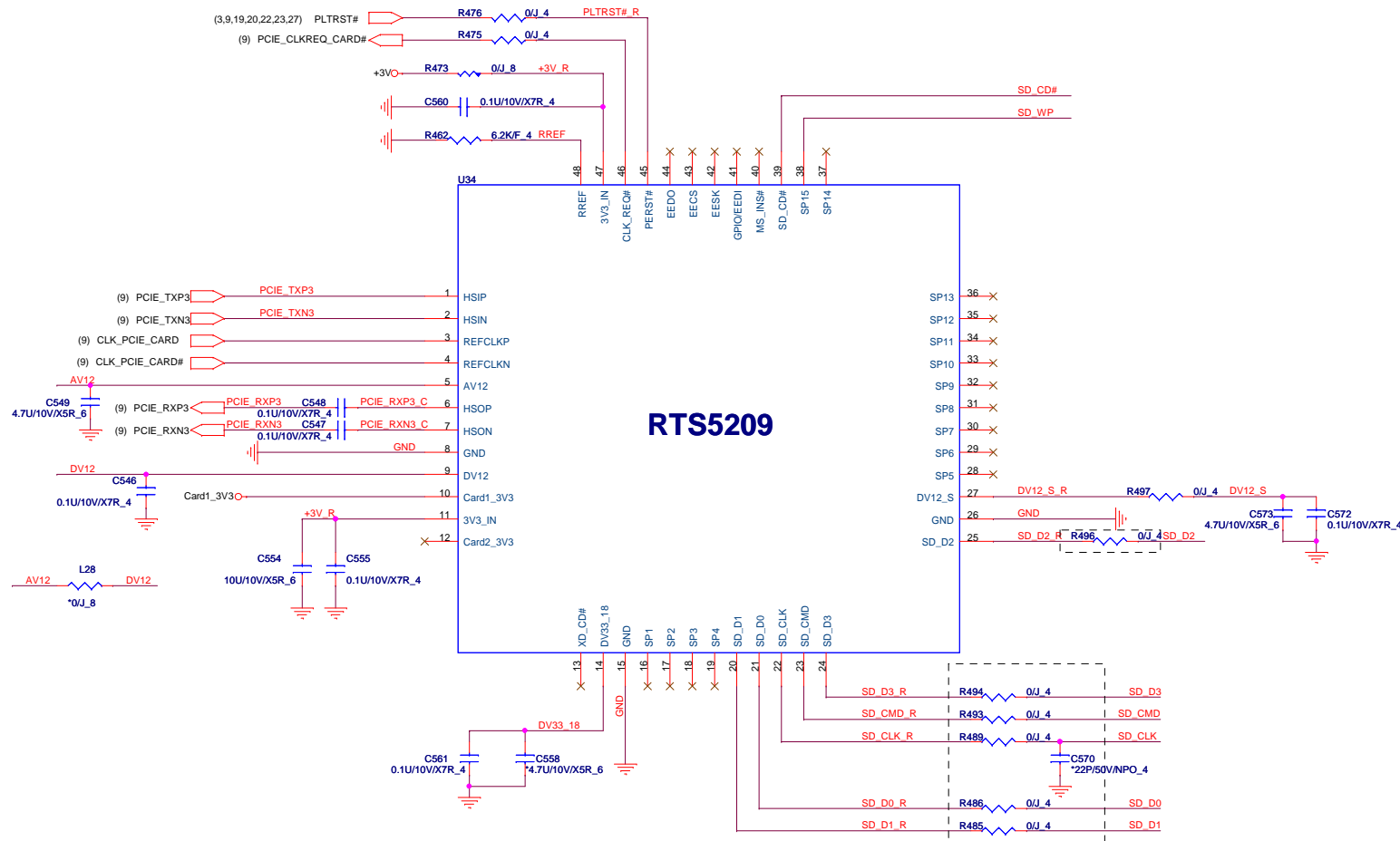


FOR EMI Reserve



Note:

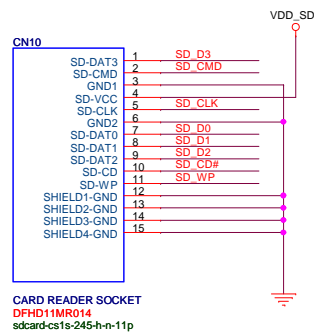
SD/MMC	MS
SP1	SD D7
SP2	SD D6
SP3	SD D5
SP4	SD D4
SP5	MS BS
SP6	
SP7	MS D1
SP8	
SP9	MS D0
SP10	MS D2
SP11	
SP12	MS D3
SP13	
SP14	MS CLK
SP15	SD_WP



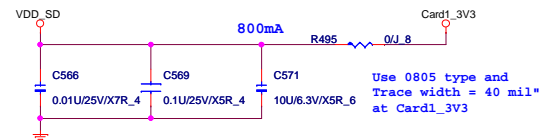
R489,R495,R499,R504,R505,R508,C568 close to chip pin

It is recommended that mismatch trace length between CLK and DATA trace is 100 mils with maximum

4 IN 1 CARD READER



Memory Card Power Supply

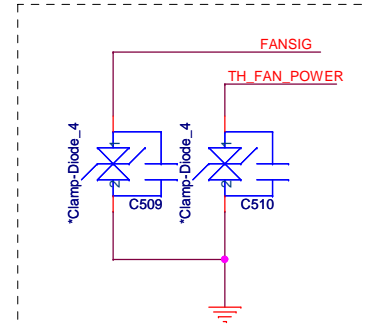
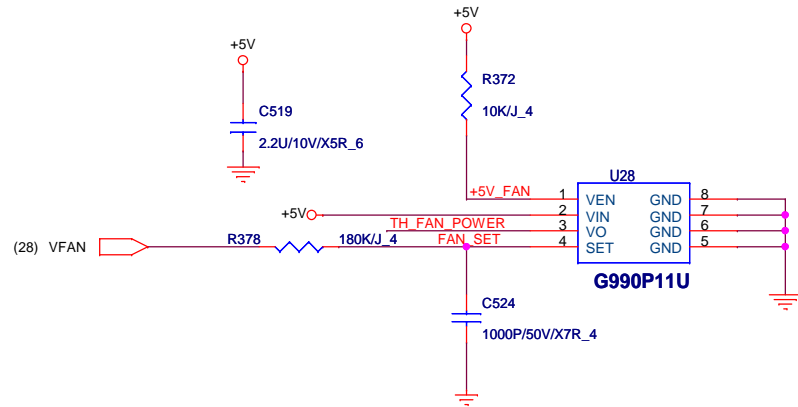


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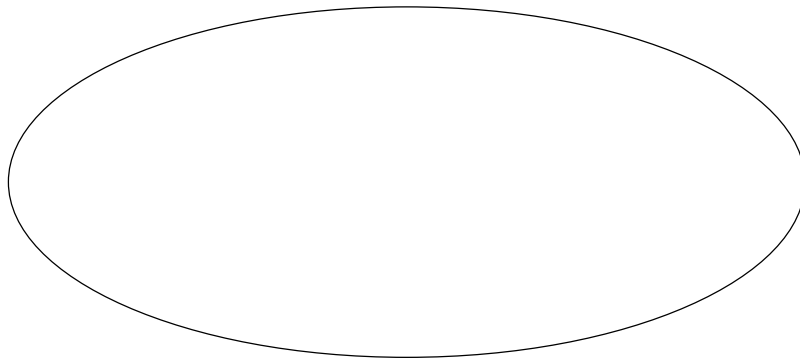
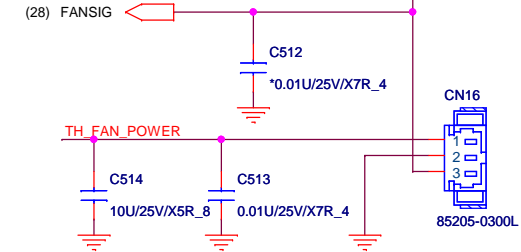
PROJECT : LI2

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FANPWR = 1.6*VSET

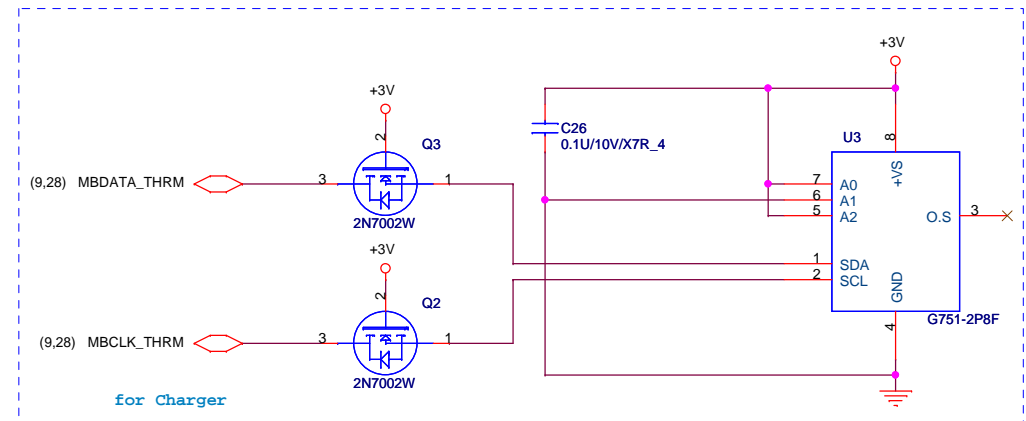


Closed to Connector
Reserved for ESD



Remove environment thermal IC

+3V (7,8,9,10,11,13,14,15,16,17,19,20,22,24,25,27,28,29,31,32,33,35,36,38,49)
+5V (8,11,16,17,21,24,29,36,38)



for Charger

ADDRESS: 9AH

ADDRESS						
1	0	0	1	A2	A1	A0
MSB				LSB		



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PROJECT : LI2

Size Document Number

FAN/Thermal

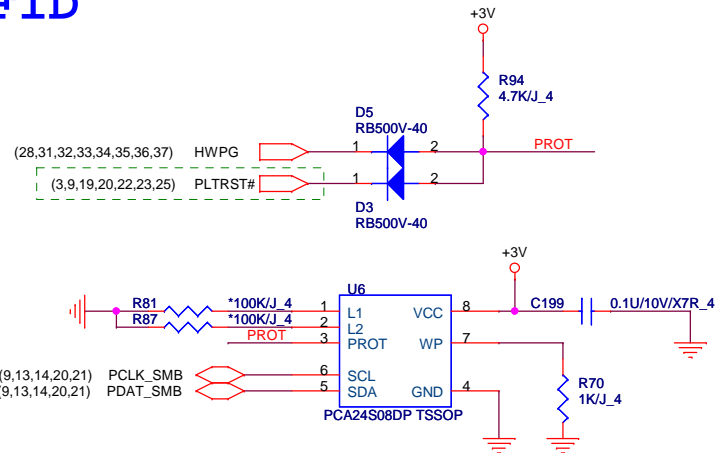
Rev

1A

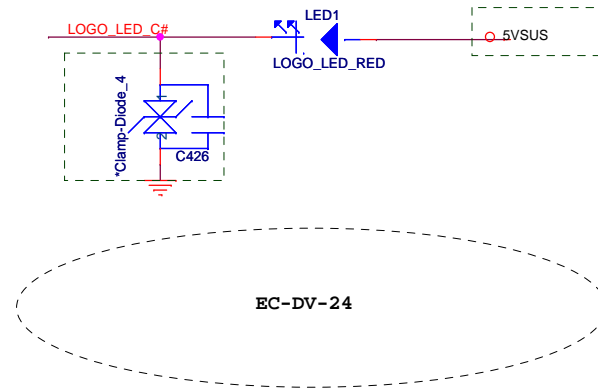
Date: Thursday, January 05, 2012

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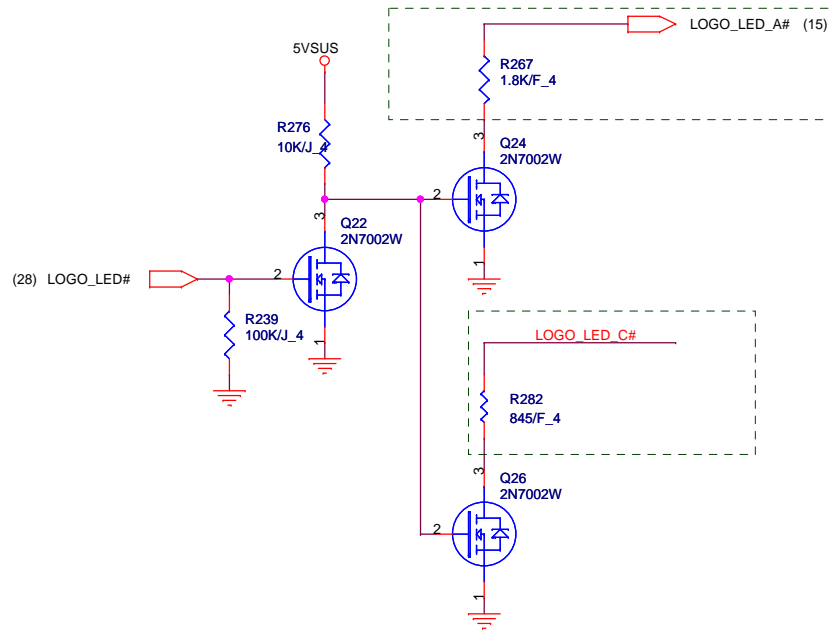
RFID



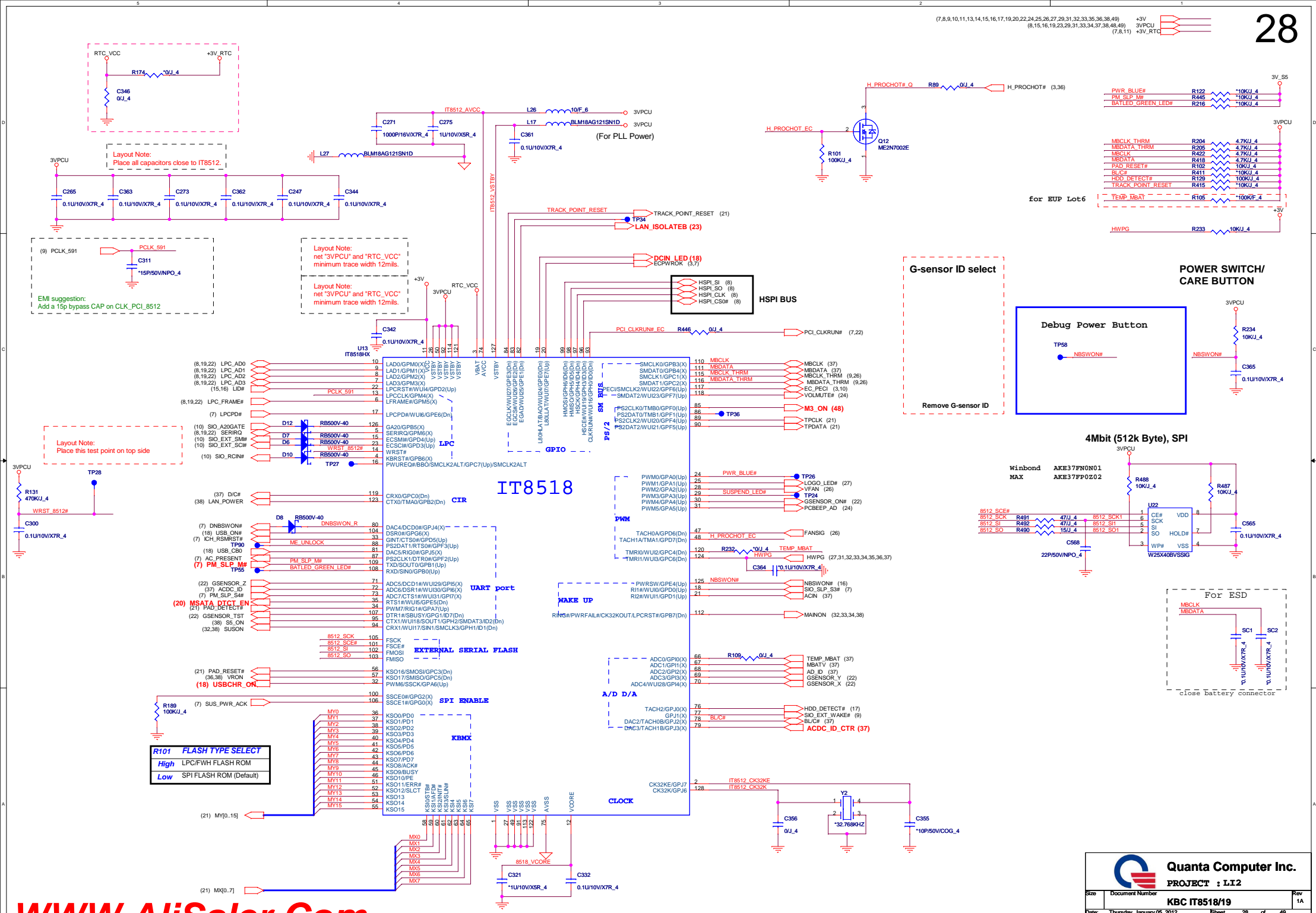
+3V (7,8,9,10,11,13,14,15,16,17,19,20,22,24,25,26,28,29,31,32,33,35,36,38,49)
 3VPCU (8,15,16,19,23,28,29,31,33,34,37,38,48,49)
 3V_S5 (3,7,8,9,10,11,19,28,38)
 5VSUS (15,38)



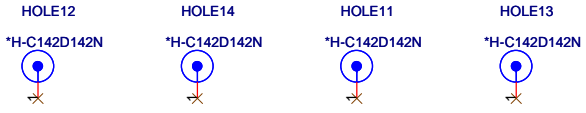
LED Driver



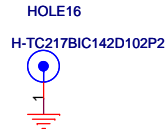
POWER BUTTON



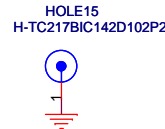
Hole for CPU support



MiniCard WWAN



MiniCard WLAN



CRT

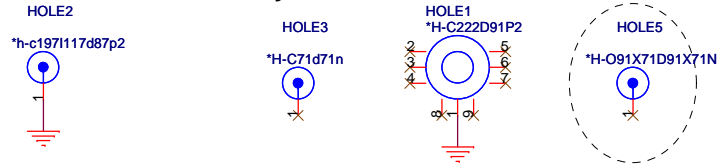


Keyboard

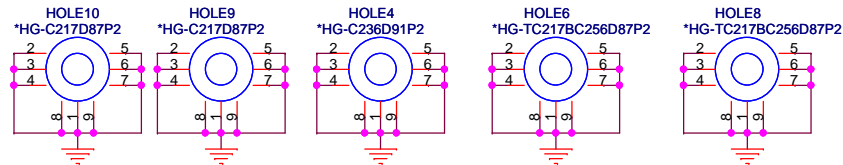


SB

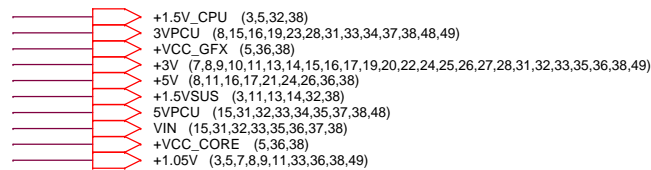
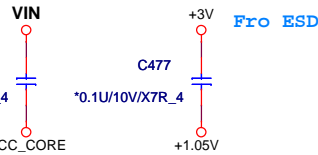
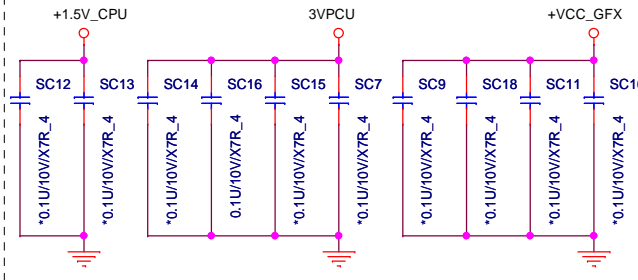
Boundary Hole



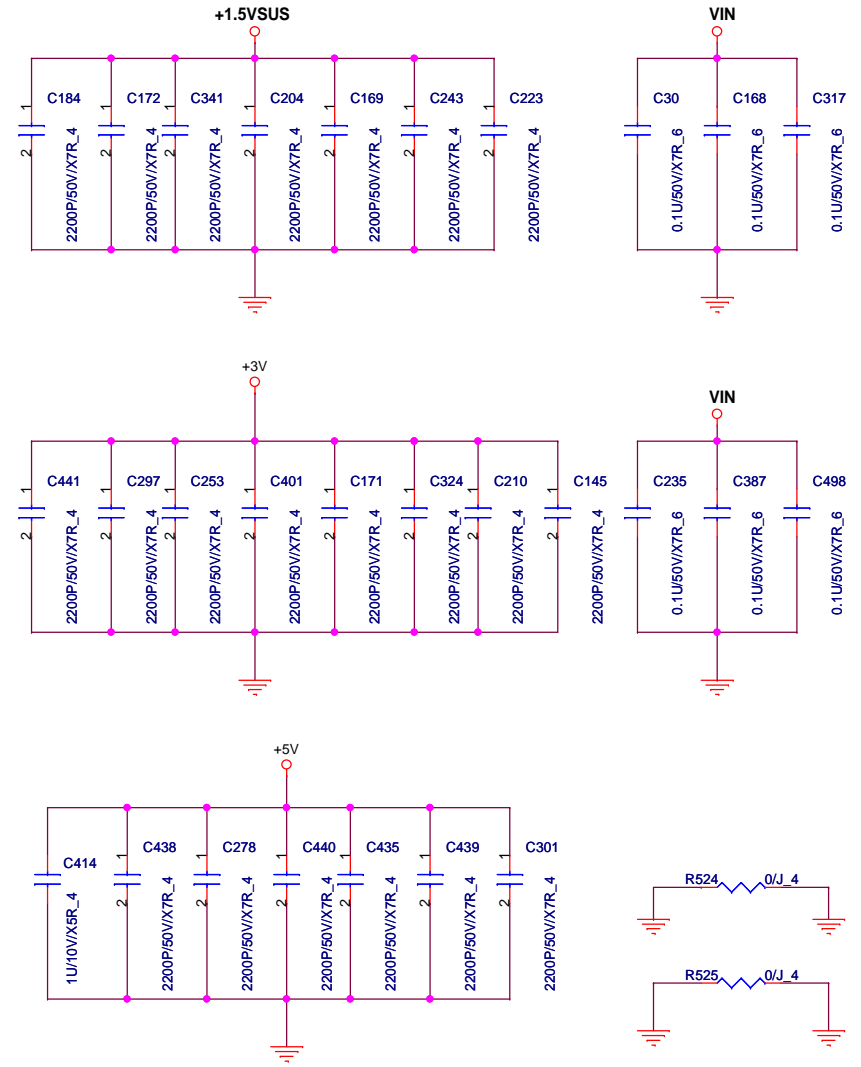
Boundary Hole



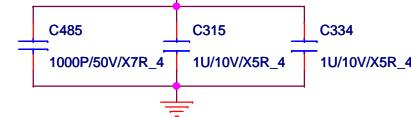
Fro ESD



EMI



Fro EMI



Quanta Computer Inc.

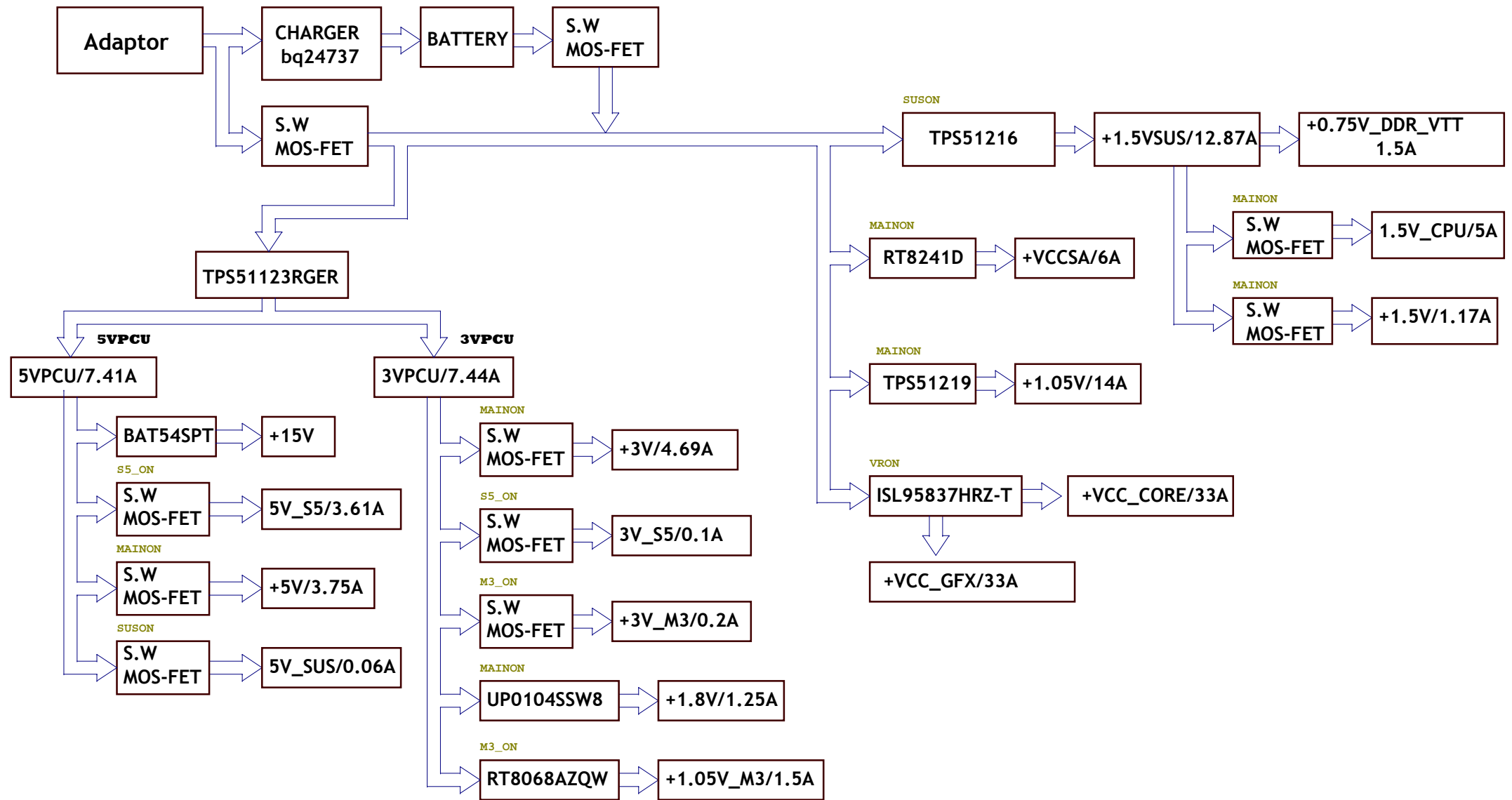
PROJECT : LI2

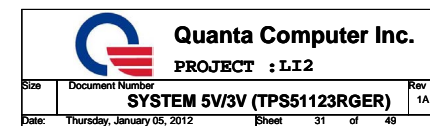
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Screw Hole/EMI

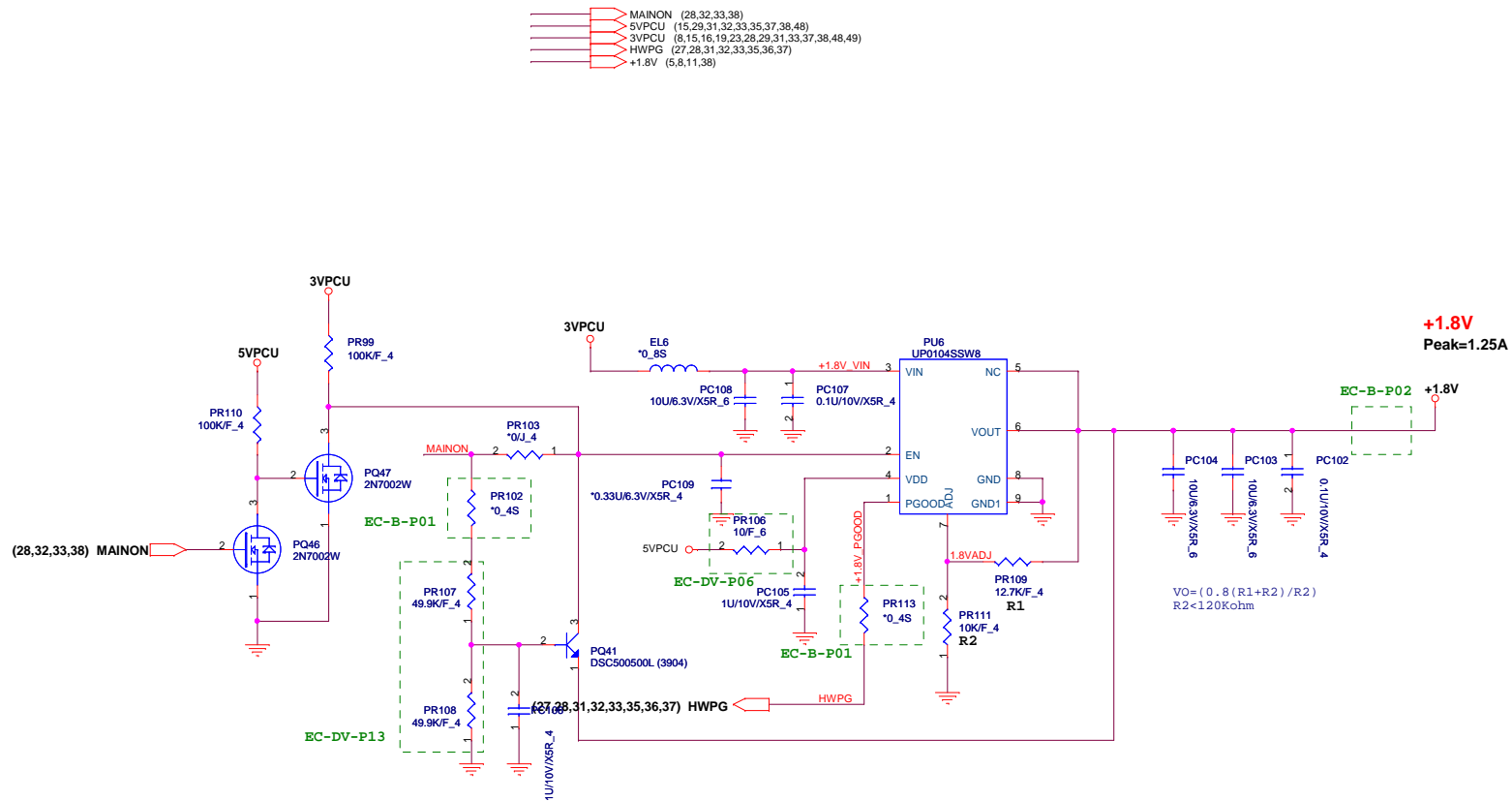
LI2 Chief River SYSTEM POWER BLOCK DIAGRAM









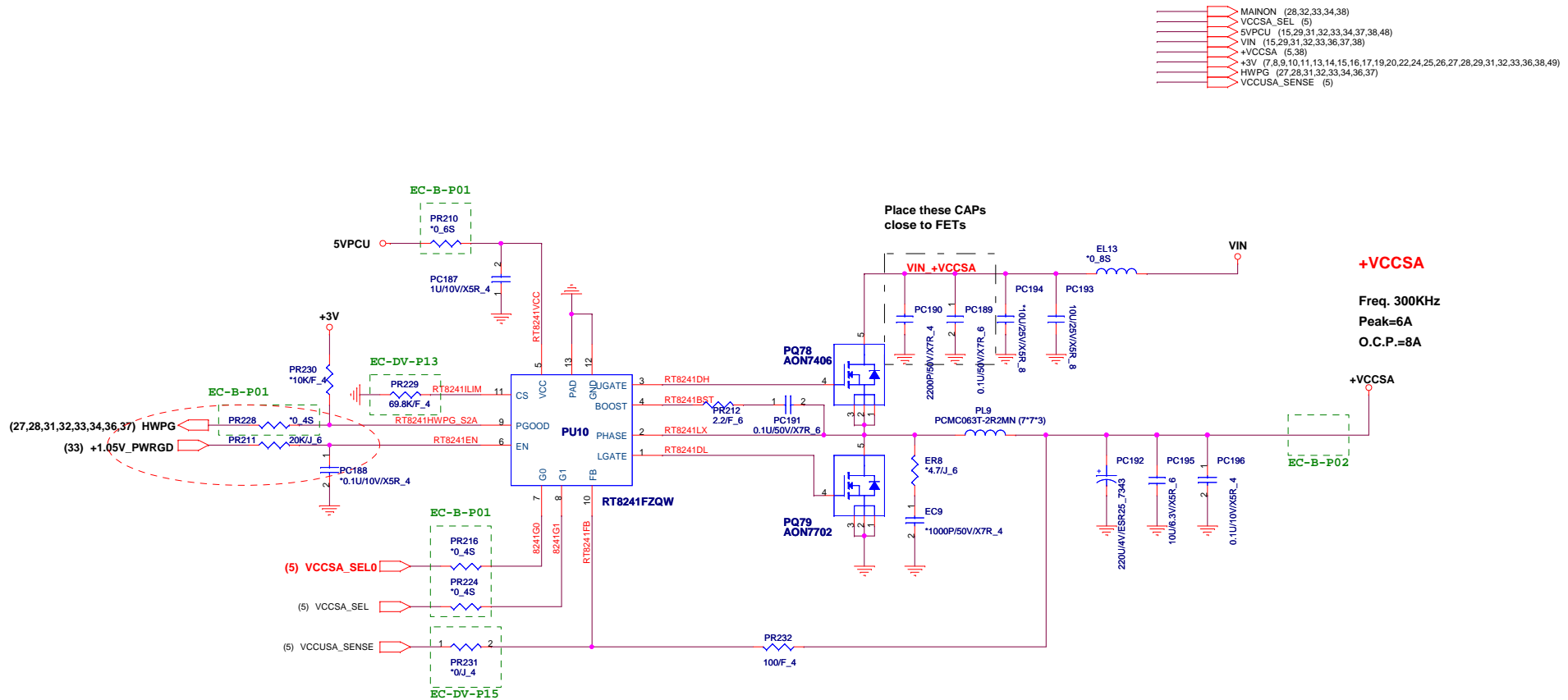


Quanta Computer Inc.

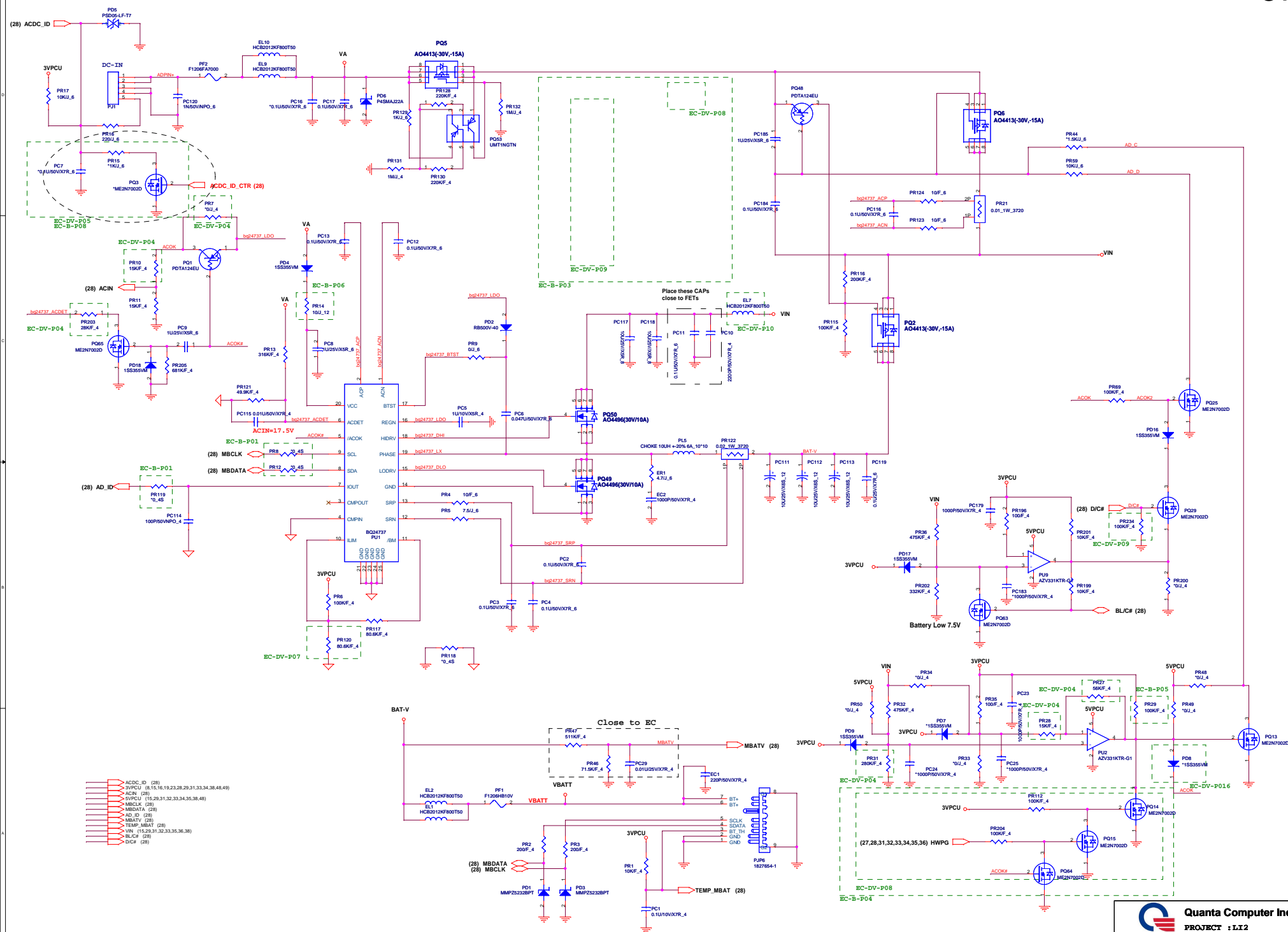
PROJECT : LI2

Size	Document Number	Rev
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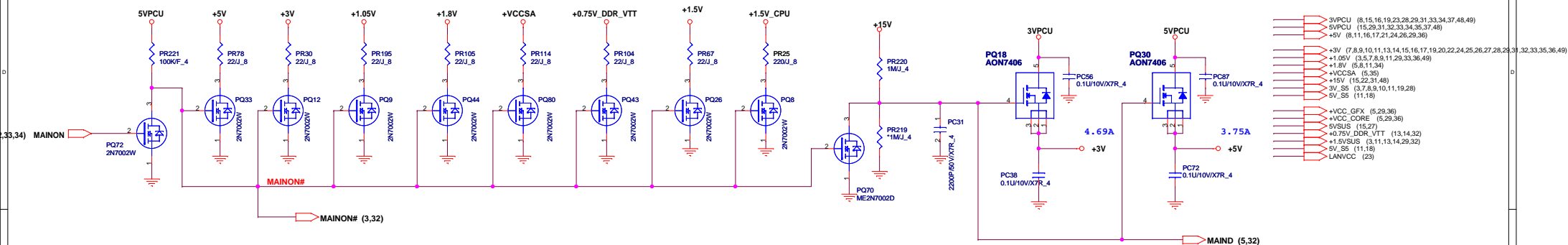
Date: Thursday, January 05, 2012 Sheet 34 of 49



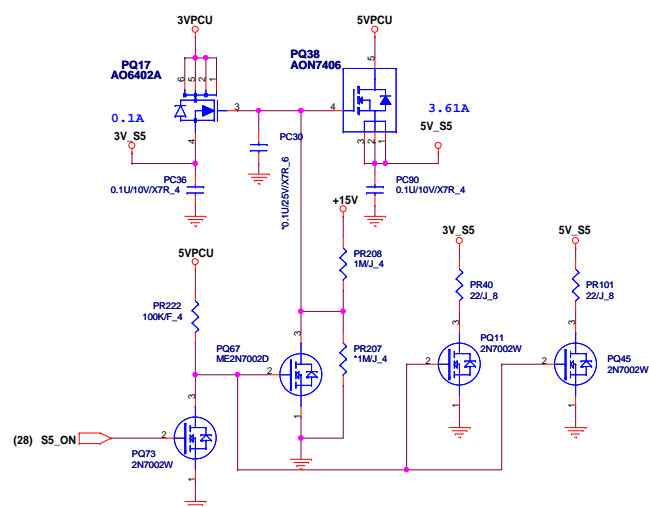
Processor	VCCSA_SELO G0	VCCSA_SEL G1	VCCSA XE&SV segments
Sandy Bridge	0	0	0.9V
	0	1	0.85V
Ivy Bridge	1	0	0.775V
	1	1	0.75V



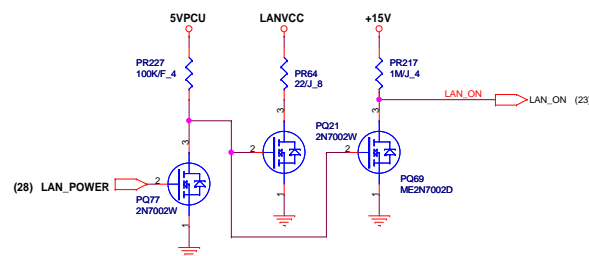
+3V, +5V, +1.05V, +1.8V, +VCCSA, +0.75V_DDR_VTT, +1.5V, +1.5V_CPU



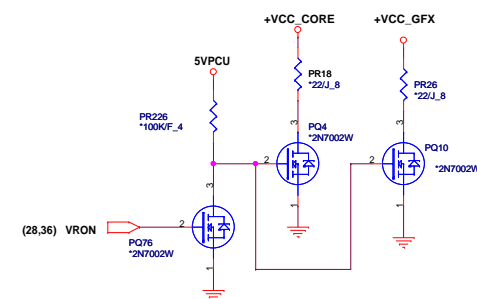
3V_S5, 5V_S5



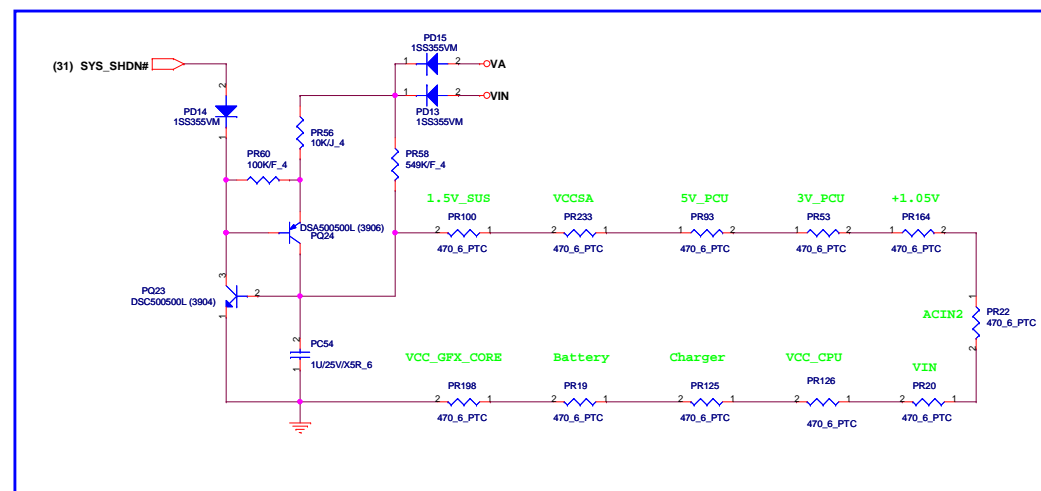
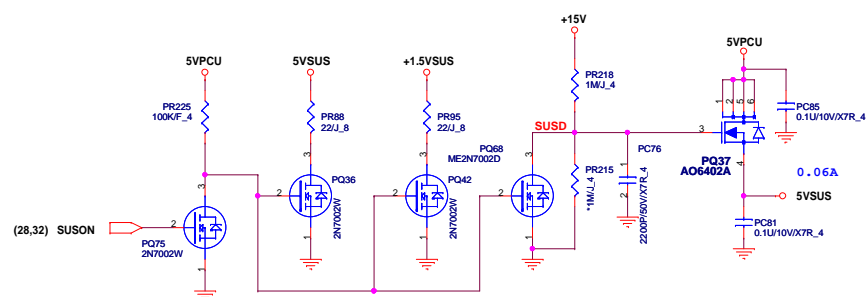
LANVCC

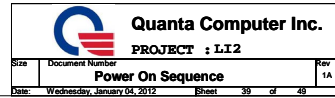


+VCC_CORE, +VCC_GFX



5VSUS, +1.5VSUS





[illegible]

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
A1A		DV	Initial release	2010/12/03	2010/12/03

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

EC #	Page	Date	Part Affected	Description
EC-DV-01	29	2011/09/07	Hole8	Remove unused Nut
EC-DV-02	15	2011/09/08	CN32	ME RECOMMAND:update CCD/LED connector for PE suggestion
EC-DV-03	16	2011/09/09	CN30	ME RECOMMAND:reverse CN30 pin define
EC-DV-04	21	2011/09/09	RV15,RV16,RV17	ESD RECOMMAND:reserve for ESD
EC-DV-05	18	2011/09/13	U43,U43	ESD RECOMMAND for layout routing:exchange USB3.0 RX and USB2.0 signal of U43 and U44
EC-DV-06	05	2011/09/13	C761,C762	Reduce for power noise:reserve C761 and C762
EC-DV-07	05	2011/09/14	C447,C59,C431,C45,C432,C430,C442,C62,C443,C56,C56,C428,C23,C49,C435,C427	Follow DG:change 15 pcs caps value from 1uf to 2.2uf
EC-DV-08	05	2011/09/14	C764,C765,C766,C767,C768,C771	Lenovo RECOMMAND :Reserve 150uF 3528 Caps of CPU Power rail
EC-DV-09	13 14	2011/09/14	C190,C191,C192,C282,C498,C499,C497,C168	Follow DG :change caps value from 1uF to 0.1uF
EC-DV-10	15	2011/09/14	CN32,C733,C734	For add new LEDs on LCO cover:update CN32 from 6 pins to 10 pins and add two Res for tuning LED brightness
EC-DV-11	19	2011/09/14	Q15,D18,R736	Remodify BT_ON schematic:Remove Q15 and add D18,R736
EC-DV-12	49	2011/09/14	Q47,Q45,R728,R727,R731	Remodify SBA schematic:Remove 1.05V_M3_PG schematic in pg49
EC-DV-13	49	2011/09/15	L51,R737	Reserve for SBA Power select
EC-DV-14	16	2011/09/16	R82,R81,R78,R77,R74,R71,R68,R62	Follow DG:update HDMI Rpd value from 499 to 680 ohm
EC-DV-15	10	2011/09/16	R738,R739	BIOS RECOMMAND:Add SBA selection schematic
EC-DV-16	05	2011/09/16	C55,C58,C429,C60,C48,C61,C445,C433,C46,C448,C439,C441,C446,C437,C47,C434,C444,C438,C440,C436	Follow DG:update +VCC_CORE caps from 1uf to 2.2uf
EC-DV-17	05	2011/09/19	R28,R29	Follow DG:update R28 and R29 Res value from 10 ohm to 100 ohm
EC-DV-18	21	2011/09/19	C772	ESD RECOMMAND:add C772 on the signal of LEFT
EC-DV-19	21	2011/09/19	C773,C774	EMI RECOMMAND:reserve for EMI
EC-DV-20	06	2011/09/19	R25,R26,R31,R30	Remove R25,R26,R31,R30
EC-DV-21	16	2011/09/19	U4,U5,U7	Add Power trace of +3V connection to pin3 of U4,U5 and U7
EC-DV-22	20	2011/09/20	RV18,RV19,RV20,RV21,RV22,U3	ESD RECOMMAND:remove U3 and RV18-RV22 for ESD solution
EC-DV-23	05	2011/09/21	C775,C776,C777,C778,C779,C780,C764,C765	No layout spacing:Remove C764 ,C765 and Add C775-C780
EC-DV-24	27	2011/09/21	LED2,R580,C383	Remove SATA LED schematic:Remove C383,R580,LED2
EC-DV-25	15	2011/09/21	Q49,Q50	Add 2 2N7002 to control CCD and WLAN LED of LCD COVER
EC-DV-26	24	2011/09/28	R268,R269,R299	FAE RECOMMAND:update PC-beeper voltage level,change R268,R269,R299 RES value form FAE suggestion

LI2 Schematic EC Tracking Record DV (for DV)XXXX. XX, 2011

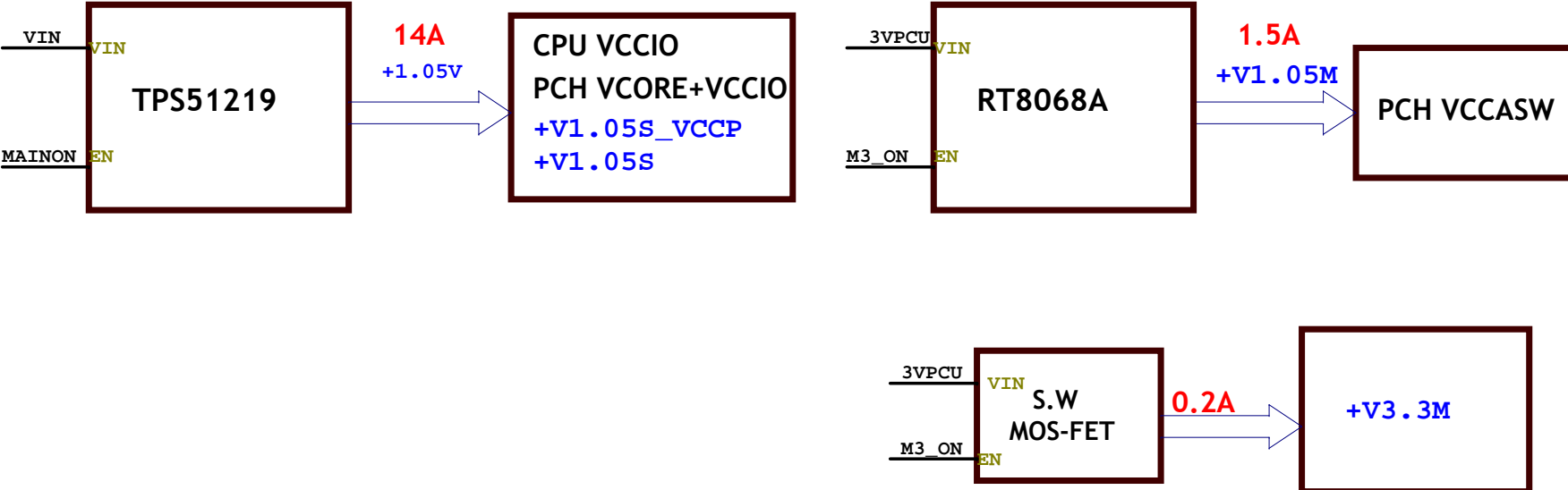
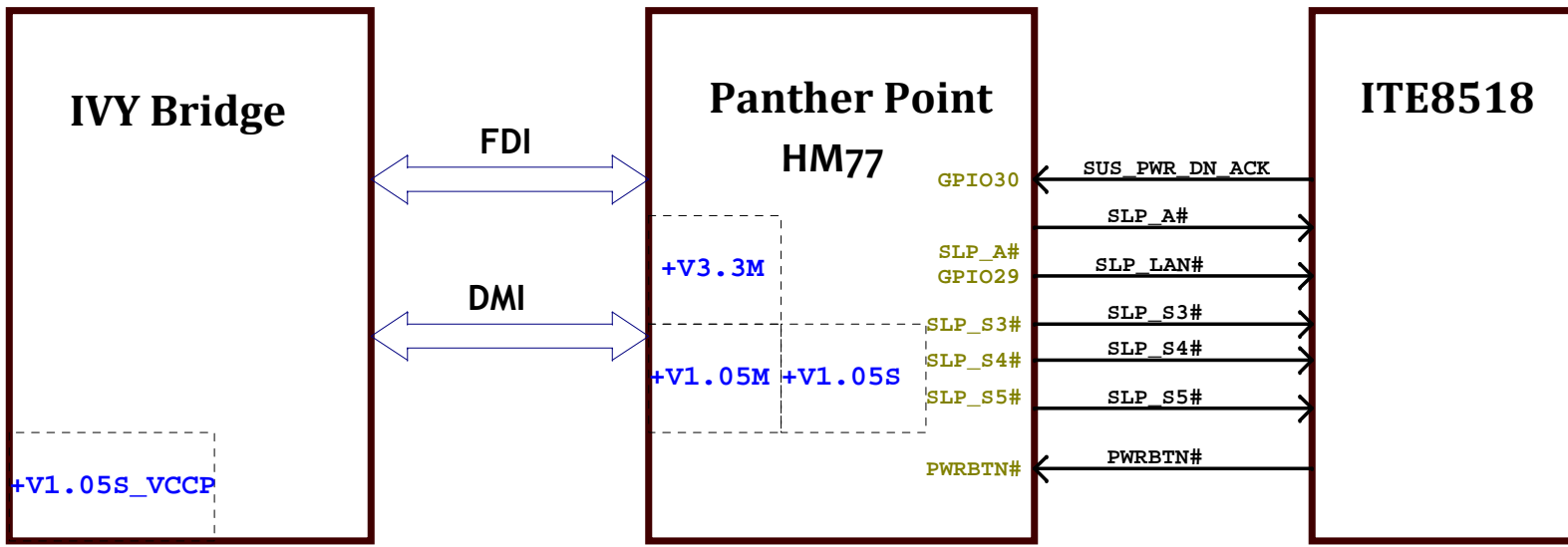
EC #	Page	Date	Part Affected	Description
EC-DV-P01	32	2011/9/7	PC99	Change for +1.05V output ripple voltage (base on TI simulation)
EC-DV-P02	31	2011/9/7	PC94	Change for 5VPCU output ripple voltage (base on TI simulation)
EC-DV-P03	36	2011/9/7	PR182, PR178, PR152	Intersil FAE recommend change value
EC-DV-P04	37	2011/9/7	PR7, PR10, PR203, PR27, PR28	TI FAE recommend change value
EC-DV-P05	37	2011/9/8	PC7, PR15, PQ3	Add for Lenovo external battery ID pin function
EC-DV-P06	34	2011/9/21	PR106	Add for uPI FAE recommend (base on uPI simulation)
EC-DV-P07	37	2011/10/3	PR120	Change for charger current limit (base on TI simulation)
EC-DV-P08	37	2011/10/3	PC186, PQ15, PR52, PD11, PC39, PR42, PQ14	Delete reserved component
EC-DV-P09	37	2011/10/3	PR234, PR235, PQ81	Add for TI FAE recommend (base on TI simulation)
EC-DV-P10	37	2011/10/3	EL7	Add for EMI team recommend (base on EMI simulation)
EC-DV-P11	36	2011/10/17	PR236	Add PR236 for DV test
EC-DV-P12	36	2011/10/17	PC161,PR186,PR183,PC163, PC146,PC137,PR150,PR159, PC135	Intersil FAE recommend change value (base on Intersil simulation)
EC-DV-P13	31 32 33 35 36	2011/10/21	PR82, PR62, PR91, PR147, PR229, PR179, PR156,PR107 PR108	Change for power converter current limit (base on OCP test)
EC-DV-P14	31	2011/10/26	PC94	change PC94 size to 3528, because orignal 3216 size has shortsge issue.
EC-DV-P15	35	2011/10/26	PR231	RT FAE recommend change to open
EC-DV-P16	37	2011/10/28	PD8	Change for DV test result (base on ACOK test)

EC #	Page	Date	Part Affected	Description
EC-B-01	03	2011/10/19	R499,R47,R43	For platforms that do not implement the S3 Power Reduction circuitry and meet Intel Power-on sequence 1.Reserve R499 on the trace of SYS_PWROK 2.R47,R469 un-mount 3.updae R43 value from 1.1k ohm to 0 ohm
EC-B-02	07	2011/10/19	R500	Reserve R500 for SBA selection and meet Intel power-on sequence.
EC-B-03	19	2011/10/19	Q42,Q43,R501	Lenovo recomment to reserve AOAC schematic: reserve Q42,Q43,R501
EC-B-04	20	2011/10/19	R502	BIOS recomment :add MSATA detect signal to GPIO27 of PCH
EC-B-05	07	2011/11/21	R83,R76	Intel recommend:HPD and HPC are active high signal,Pull ups are not required for unused ports:R83 and R76 are un-mounted
EC-B-06	03	2011/11/21	R346	Intel recommend:if eDP is not used EDP_HPDP can be left as unconnected.R346 un-mounted
EC-B-07	11	2011/11/21	R208,R241,L18	Intel recommend:3VS_VCC_CLKF33 filter is no longer required. Keep the Cdecap, but remove the Cfilter/Lfilter. CRB schematics includes these components but they are not required on customer designs:R208 mountrd and R241,L18 are un-mounted
EC-B-08	16	2011/11/21		To support DC mode S4 wake up from LCD,update Lid switch power rail from 3V_S5 to 3VPCU
EC-B-09	15	2011/11/21		Camera VCC power rail issue:change the power rail from +5V to +3V
EC-B-10	09	2011/11/28	Q19,Q20	Reduce 3V_S5 leakage:SWAP the signals pin1 and pin3 of Q19 and Q20
EC-B-11	10 15	2011/11/28	Q44~Q47,R507	Lenovo recoomand to verify RF LED function:Add Q44~Q47 ,R507 and modify WWAN_LED_ON to GPIO16 of PCH
EC-B-12	16	2011/11/28	D18,D19,R504,R505	Reduce +5V leakage from HDMI device:Add D18,D19 ,R504 and R505
EC-B-13	16 18	2011/11/28	SU1~SU7	ESD recommend:update ESD protection component of SU1~SU7 to HDMI and USB3.0 sginals
EC-B-14	19 20	2011/11/28	CN21,CN22	Layout recoomend:update minipcie footprint to minipci-aaa-pci-041-k01-52p-smt
EC-B-15	49	2011/11/28	R506 ,C574	To fine tuning Intel Power-on sequence:Add RC delay of ACPWROK add R506 and C574
EC-B-16	10	2011/11/28		Intel recommend:GPIO36 and GPIO37 should not be pulled high when strap is sampled.Change Jett/Dutton strap pin to GPIO38

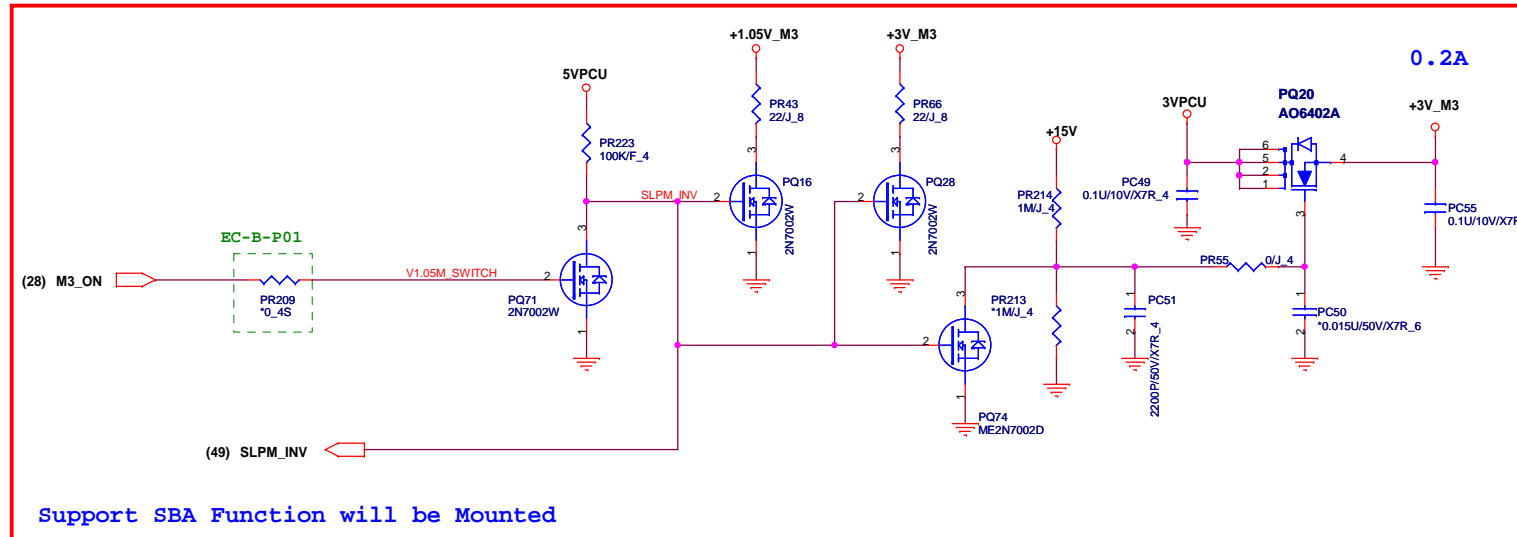
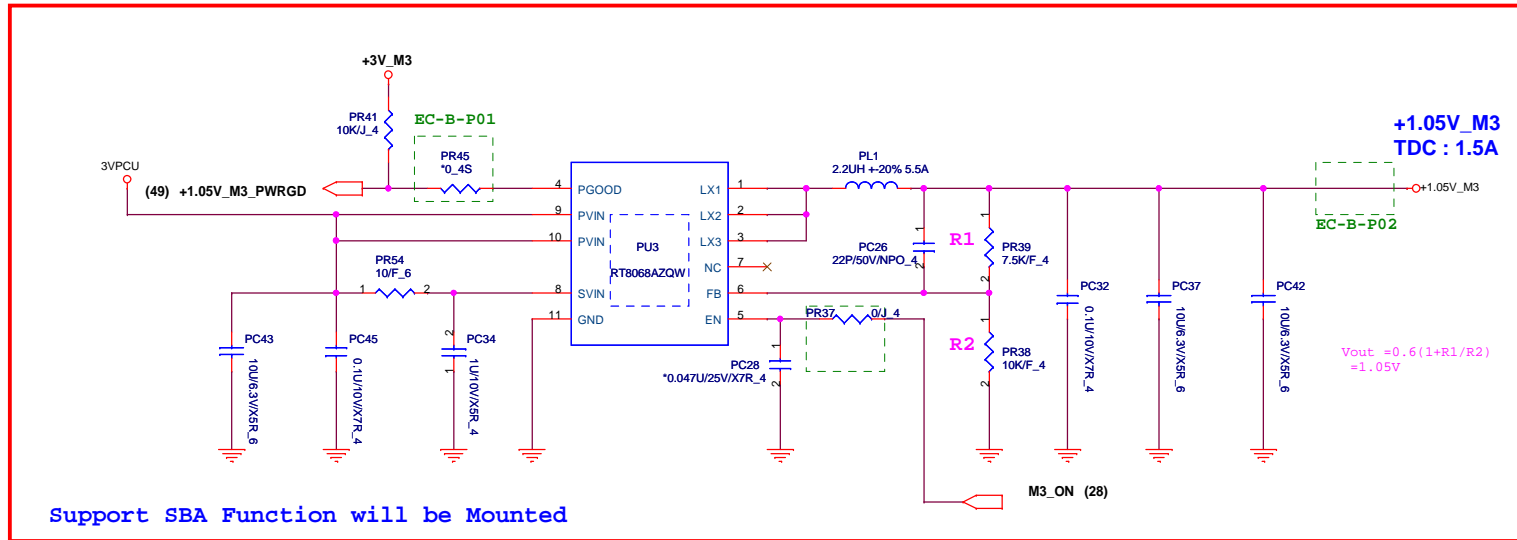
LI2 Schematic EC Tracking Record B 11.22.2011

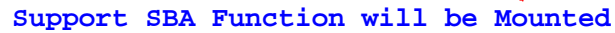
EC #	Page	Date	Part Affected	Description
EC-B-P01	31~37 48	2011/11/22	PR71, PR77, PR157, PR57, PR210, PR161, PR173, PR74, PR81, PR209, PR86, PR119, PR12, PR8, PR24, PR70, PR135, PR133, PR137, PR138, PR151, PR102, PR113, PR37, PR45, PR75, PR89, PR90, PR172, PR171, PR169, PR216, PR224, PR228, PR65	Change 0 ohm (for DV test) to short Pad
EC-B-P02	32 33 34 35 48	2011/11/22	PJP2, PJP3, PJP4, PJP7, PJP8, PJP9, PJP5, PJP10 PJP1	Remove Jump for C stage
EC-B-P03	37	2011/11/22	PQ64, PR204, PQ66, PR235, PQ81	Delete reserved component
EC-B-P04	37	2011/11/22	PR112, PQ14, PR204, PQ15, PQ64	Add for TI FAE recommend (base on DV test)
EC-B-P05	37	2011/11/22	PR29	Change PR29 form 10K to 100K (base on DV test)
EC-B-P06	37	2011/11/23	PR14	Change PR14 form 0603 size to 1206 size (base on TI simulation)
EC-B-P07	31	2011/11/24	PC78	Change PC78 form de-pop to pop (base on DV test)
EC-B-P08	37	2011/12/02	PC7,PR15,PQ3	Because we don't need to support the external Battery PC7,PR15,PQ3 un-mounted

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+3V_M3 (8,11,23,49)
+1.05V_M3 (11,49)





EC-DV-13

EC-DV-12

Support SBA Function will be Mounted

Support SBA Function will be Mounted

Support SBA Function will be Mounted